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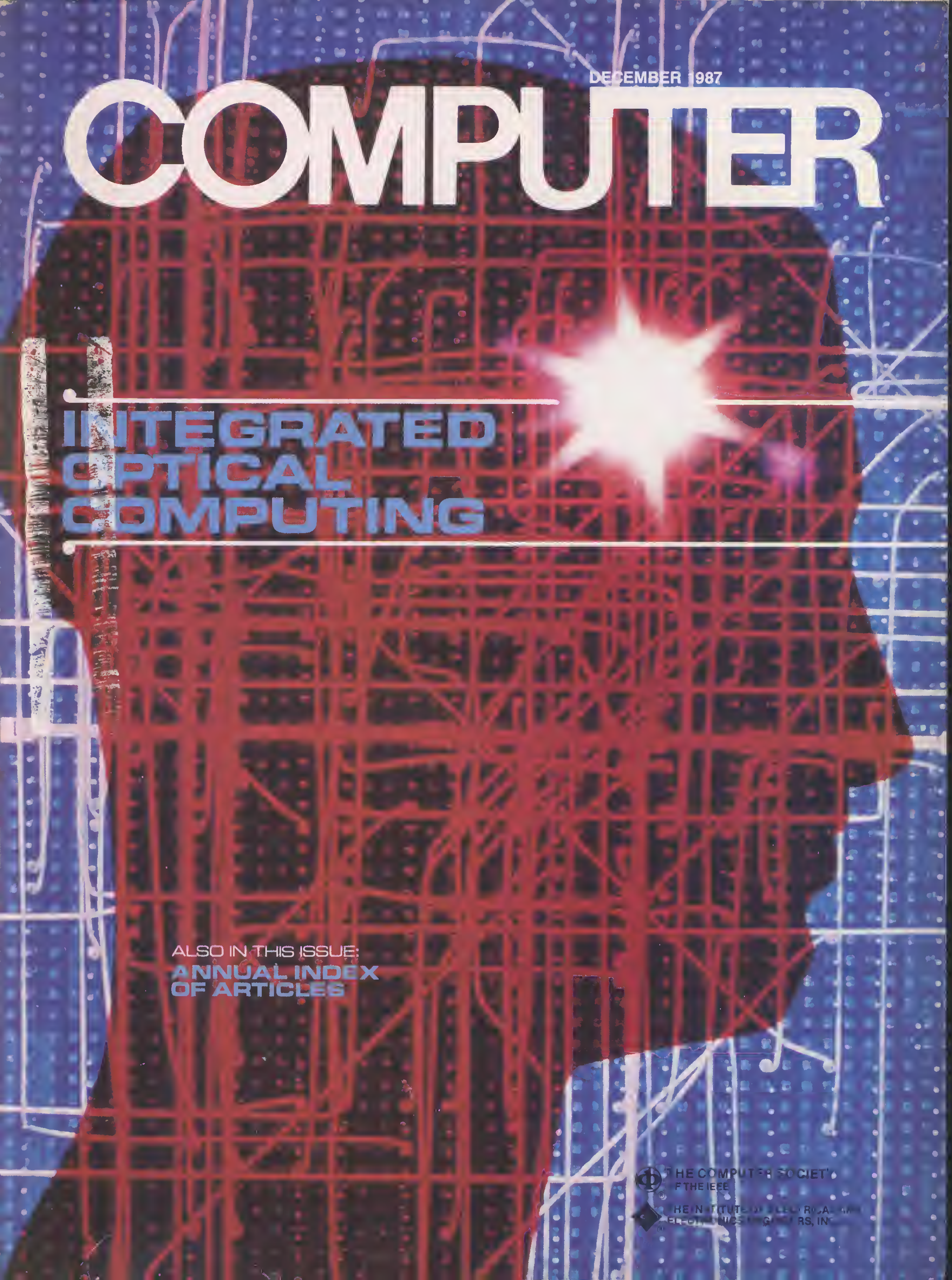

INTEGRATED OPTICAL COMPUTING

ALSO IN THIS ISSUE:
ANNUAL INDEX OF ARTICLES

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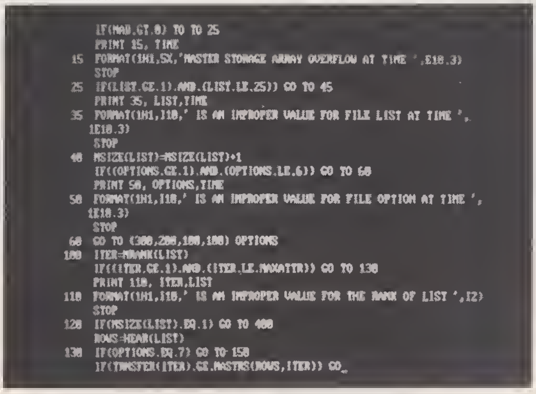
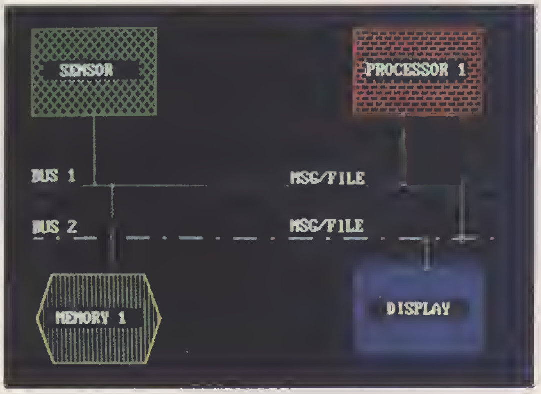


```
      IF(NAB.GT.0) TO TO 25
      PRINT 15, TIME
 15   FORMAT(1H1,5X,'MASTER STORAGE ARRAY OVERFLOW AT TIME ',E10.3)
      STOP
 25   IF(LIST.GE.1).AND.(LIST.LE.25)) GO TO 45
      PRINT 35, LIST,TIME
 35   FORMAT(1H1,I10,' IS AN IMPROPER VALUE FOR FILE LIST AT TIME ',
     1E10.3)
      STOP
 40   MSIZE(LIST)=MSIZE(LIST)+1
      IF((OPTIONS.GE.1).AND.(OPTIONS.LE.6)) GO TO 60
      PRINT 50, OPTIONS,TIME
 50   FORMAT(1H1,I10,' IS AN IMPROPER VALUE FOR FILE OPTION AT TIME ',
     1E10.3)
      STOP
 60   GO TO (300,200,100,100) OPTIONS
100   ITER=MRANK(LIST)
      IF((ITER.GE.1).AND.(ITER.LE.MAXATTR)) GO TO 130
      PRINT 110, ITER,LIST
110   FORMAT(1H1,I10,' IS AN IMPROPER VALUE FOR THE RANK OF LIST ',I2)
      STOP
120   IF(MSIZE(LIST).EQ.1) GO TO 400
      NOWS=MEAN(LIST)
130   IF(OPTIONS.EQ.7) GO TO 150
      IF(TRNSFER(ITER).GE.MASTRS(NOWS,ITER)) GO_
```

Costs and delays of programming

AFTER



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COMPUTER

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BPA

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LETTERS TO THE EDITOR

Language level critical for DSI and function points

To the editor:

In Barry Boehm's otherwise excellent article, ''Improving Software Productivity,'' in the September issue of *Computer*, the discussion on delivered source instructions (DSI) as a productivity metric unfortunately omits the primary weakness of DSI; that is, it tends to move backwards as economic productivity improves.

Domains outside of software have recognized for more than 200 years that if a manufacturing process involves a significant amount of fixed costs, and there is a reduction in the number of units manufactured, then the cost per unit must go up.

A significant proportion of software development costs are either fixed or inelastic, in that they do not relate in any way to DSI. Activities such as requirements, initial design, architecture, user documentation, and design reviews stay essentially constant regardless of DSI, and the costs of these activities range from 35 percent to more than 60 percent of the total cost of a large software system. Coding itself and code-related costs may total less than 25 percent of all development—especially for large military projects following military specifications, with their enormous paperwork requirements.

DSI originated in the early days of software when coding was the primary task and code was the primary deliverable. Since the early 1970s, coding itself has dropped in overall percentage of costs while paperwork has expanded. Clearly, DSI is not a suitable metric for paper-intensive activities.

To illustrate the paradoxical regression of DSI as a productivity metric, consider the results of two similar projects in terms of functionality, with one of the projects being written in Macro Assembler and the second in Ada (see table).

Clearly, neither DSI per man-month nor cost per source statement match the economics of the situation—a two to one improvement in economic productivity on the side of Ada.

In this example, the IBM function-point technique developed by A.J. Albrecht gives a much better fit to economic productivity than DSI.

Boehm correctly points out that the function point method itself is not completely error-free, and many of the terms are ambiguous and prone to varying interpretations. In my own side-by-side measurements of software projects, I record both the DSI and function point sizes and also the counting rules in effect. My observations indicate errors in excess of 800 percent in counting DSI but only 200 percent in counting function points. Unlike DSI, which has remained unstandardized for more than 40 years, function points has an active forum of users (the International Function Point Users' Group) and a much better prognosis for achieving a satisfactory level of consistency than DSI has ever had.

Software productivity rates measured with DSI have exhibited the largest variation of any human activity. Much of that variation is spurious and attributed to the paradoxical behavior of the DSI metric itself. Careful side-by-side measurements of projects with both function points and DSI are starting to favor function points for consistency, and certainly for coming to grips with economic productivity.

Capers Jones
Software Productivity Research, Inc.

Project comparison

	Macro Assembler Version	Ada Version
Source code size	70,000 DSI	25,000 DSI
Development costs	$1,043,000	$590,000
DSI per man-month	335	211
Cost per source statement	$14.90	$23.60
Function point per man-month	1.65	2.92
Cost per function point	$3,023	$1,710

Author's reply:

Capers Jones' letter makes some very good points. Comparing productivity rates in DSI across different language levels (assembly, Ada, fourth-generation languages) does not make much sense. DSI users need to account for their language levels to avoid the paradoxes shown in Jones' letter. In general, organizations can avoid seriously misleading themselves by adopting a guideline of not using a lower level language where a higher level language can do the job.

For all their good aspects, function points have their paradoxes as well. A common example involves software maintenance, where one can make a lot of useful changes to a program's code without making any change in its inputs, outputs, etc. Thus, there is no change in function points, and one gets no productivity credit at all.

All of this points to the need for caution in interpreting productivity figures and for further experimentation and careful definition in the area of software productivity metrics.

Barry W. Boehm
TRW Defense Systems Group

Letraset pricing clarified

To the editor:

On p. 90 of the October issue of *Computer* ("Letraset upgrades design software"), you state that ImageStudio, Letraset's new image processing software for the Macintosh, costs $495 and is available to registered Ready Set Go! users for $75. The suggested retail price of ImageStudio is $495, as stated.

However, there is no special offer whereby registered Ready Set Go users can purchase ImageStudio for $75. I hope this will clarify our pricing for your readers.

Michael Rennert
Letraset USA

Abstract data types here to stay

To the editor:

Although you have, no doubt, received several letters in the same vein, the following point is so important that I cannot in conscience leave the task to those of a like mind and risk that everyone else also defer.

I am thankful that the authors of "The Effect of Abstract Data Types on Program Development" (Jeffrey Mitchell, Joseph E. Urban, and Robert McDonald, *Computer*, August 1987, pp. 85-88) did not suggest that we abandon abstract data types altogether, but one could infer from the conclusion in their article that if one lacks an automatic ADT generator (to presume that such an animal exists!), then one should avoid the use of ADTs in programming. I assert that such an idea is penny-wise and pound-foolish.

It is certainly beyond the scope of their study to discover the true value of ADTs. Since coding constitutes just a small portion of the software life cycle, they leave unexplored the possibility that the code written with the use of ADTs will be more maintainable, more extensible, and easier to analyze and reuse in other applications. One ADT module, properly written, can be employed in a whole raft of applications, and even several times within one application. The whole idea of keeping the data type as abstract as possible (while still exhibiting its defining characteristics) makes this reuse possible.

Perhaps the time spent by the ADT team on programming the ADT portion of the project should be amortized over a dozen or so hypothetical future applications. In that case, I have no doubt that the ADT team would emerge as the true winner in this contest.

Thomas H. Hildebrandt
Raleigh, N.C.

Author's Reply:

We agree that abstract data types positively affect much of the software development and maintenance process, and we do *not* suggest abandoning abstract data types. Our empirical evidence shows that the additional effort necessary to implement abstract data types prolongs the development effort. As Thomas Hildebrandt suggested, this development cost could be amortized over several projects, provided the supporting code for the abstract data types was generic enough to be used in the different applications.

It is apparent that the development effort can be streamlined if the implementation of the abstract data type is somewhat independent of the project's coding phase. This can be accomplished either by generating the abstract data types automatically (B. Belkhouche and J.E. Urban, "Direct Implementation of Abstract Data Types from Abstract Specifications," *IEEE Trans. Software Eng.*, May 1986, pp. 649-661) or by implementing the abstract data types independently.

Jeffrey Mitchell
University of Southwestern Louisiana

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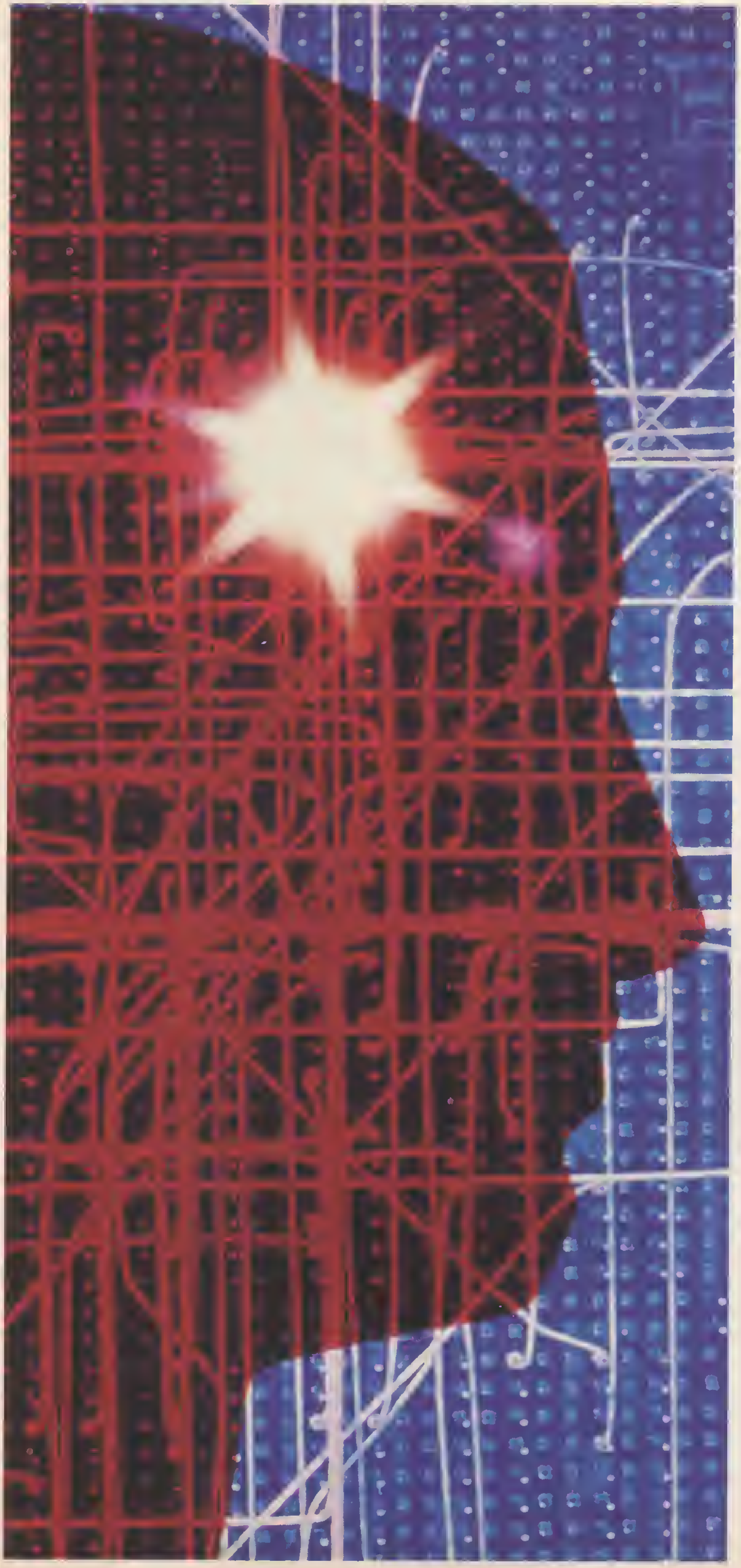

Guest Editors' Introduction

Integrated Optical Computing

T. E. Batchman
University of Virginia

Edward A. Parrish, Jr.
Vanderbilt University

In reading this introduction, you are using the most sophisticated integrated signal processing and computing system known. This system has multiple types of sensors, with a highly developed local area network connecting to a processor that has yet to be understood and is unlikely to be duplicated. One of the key features of the human vision-knowledge system is the integration achieved using common biological building blocks. Because of this integration, we are able to sense information from multiple sources, make decisions, and transmit control signals in periods of time ranging from fractions of a second to seconds.

A number of scenarios can be developed that require instantaneous processing of vast amounts of information, which may be changing radically from moment to moment. One of these scenarios is the National Aerospace Plane being studied by NASA, in which information from many sensors must be transmitted, processed, and acted upon within seconds. This challenge has been presented to

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Integrated optical computing is a promising new technology. The potential exists for a major impact on future generations of computing equipment.

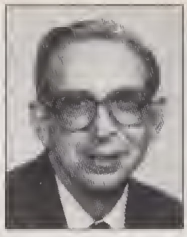
researchers in the optical computing field. As Trudy E. Bell pointed out in the August 1986 *IEEE Spectrum,* "A worldwide race is on to develop machines that compute with photons instead of electrons—but what is the best approach?"

In this issue of *Computer*, we will explore an approach that focuses on the integration of photonic devices on a common substrate. The advantages of integration in optical signal processing and computing are much the same as those realized with integrated electronics. These include compactness, insensitivity to shocks and vibrations, reduced cost, uniformity, ruggedness, and reliability. Researchers in at least 10 countries are working on integrated optical and integrated optoelectronic devices and technologies. A recent survey of 23 experts conducted by SEAI Technical Publications of Madison, Ga., predicts an annual market for optical computing devices and systems in excess of $1 billion by the year 2000. J.R. Ryan of ElectroniCast predicts a worldwide consumption of integrated optoelectronic circuits of $106 million in 1991 and $930 million by 1997. Many of those integrated optoelectronic devices will be employed in optical computers.

Integrated optics may be defined as the subfield of optics concerned with monolithic, integrated devices incorporating active and passive optical, electro-optical, acousto-optical, and electronic circuits on a suitable substrate. A few of the functions that may be integrated on a single substrate include light generation, photodetection, reflection, memory, light waveguiding, modulation, switching, amplification, beam forming, and Fourier transforming. One problem with integration of these functions is that most of the devices available today require different substrate materials ranging from glasses to compound semiconductors. There is no single optical material that has the properties silicon offers to electronic devices. Many researchers would argue that gallium arsenide (GaAs) will become the material of choice for integrated optics, since light sources are readily fabricated by various techniques on this direct bandgap material.

In 1965, a group at Bell Laboratories formulated a scheme for the use of thin-film and photolithographic techniques for the production of optical waveguide devices of various types. It was not until 1969, when the *Bell System Technical Journal* devoted an issue to the subject and coined the term integrated optics, that the field began to grow rapidly. Although research and development efforts are currently being pursued in more than 50 laboratories at governmental agencies, industries, and universities, progress over the past 15 years has been slow. This slow progress has been due in part to the lack of the same driving forces that have propelled the microelectronics industry for the past 30 years. Additionally, since many system designers are not accustomed to optical techniques, there has not been the same market push in the photonics area. Even today, with the widespread use of optical fibers, optics is often viewed as an unproven technology.

The real push in integrated optoelectronics has come from Japan. In the late 1970s, the Optical Measurement and Control Project was founded, uniting 14 companies and institutes in an effort directed at the realization of optical components using GaAs technology. Two years ago, a Japanese group presented a prototype for the complete optical train of an optical disk player on a single substrate having only the diode laser source as a discrete component. This could well be the commercial market demand necessary for development of a variety of new circuits. Integrated optical spectrum analyzers have provided the defense system designer with a new device for rapid signal analysis that cannot be electronically duplicated. Add to these facts the recent announcements of low threshold current quantum-well lasers capable of being driven directly by logic level signals, and we have the beginning of an exciting new technology that will undoubtedly impact future generations of computing equipment. □



T.E. Batchman has been a professor on the faculty of the Electrical Engineering Dept. of the University of Virginia, Charlottesville, since 1975. His research activities include integrated optical devices, microwave sensors, fiber optic sensors, and optical computing. Previously, he was an electro-optics engineering scientific specialist with LTV Missiles and Space Division; and a member of the faculty of the University of Queensland in Brisbane, Australia, where he was a senior lecturer. Among his research activities at the university were integrated and fiber optics, and dynamic modeling of telecommunications systems.

Batchman received the BSEE, MSEE, and PhD degrees in electrical engineering from the University of Kansas in 1962, 1963, and 1966, respectively.

He is a senior member of the IEEE, and a member of Eta Kappa Nu, Sigma Tau, Tau Beta Pi, and Sigma Xi.

Readers may write to Batchman at the Electrical Engineering Dept., University of Virginia, Charlottesville, VA 22901.

Edward A. Parrish, Jr., has been centennial professor of electrical engineering and dean of the School of Engineering at Vanderbilt University since January 1987. His research interests lie in the areas of pattern recognition and image processing. Previously, Parrish served as chairman of the Dept. of Electrical Engineering of the University of Virginia from 1978 to 1986. He joined the department in 1968.

Parrish is a fellow of the IEEE, a member of Tau Beta Pi, Eta Kappa Nu, Sigma Xi, and the Pattern Recognition Society, and a licensed professional engineer in Virginia and Tennessee. He has been especially active in the Computer Society of the IEEE, holding numerous offices and committee memberships. He is currently president-elect and will assume the office of president in January 1988.

He received the BEE, MEE and ScD degrees from the University of Virginia, Charlottesville, in 1964, 1966, and 1968, respectively.

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- *DEVELOPMENTS IN INTEGRATED DEVICE TECHNOLOGIES* by MIKE CALLAHAN
- *UPDATE ON RISC ARCHITECTURE* by JOHN HENNESSY
- *DEVELOPMENTS IN NEURAL NETWORKS* by FEDERICO FAGGIN

NEW EMERGING PROCESSOR ARCHITECTURES:

- SPARC
- TRON
- AT&T 32200
- NEC V60/V70
- REGULUS
- NS 32532

RECENT DEVELOPMENTS IN WORKSTATIONS AND THE EMERGENCE OF THE PERSONAL SUPERCOMPUTER:

- SUN-4
- SONY NEWS
- APOLLO
- DANA
- STELLER
- SILICON GRAPHICS

THE LATEST IN MINI SUPERCOMPUTER DEVELOPMENTS:

- CYDROME
- SEQUENT
- SUPERTEK

THE COMEBACK OF NEURAL NETWORKS

NEW STORAGE TECHNOLOGIES: **MAGNETIC OPTICAL CACHING**

COMPUTER AIDED SOFTWARE ENGINEERING **CASE**

NEW STANDARDS: **VHDL EDIF**

LEGAL ISSUES: SOFTWARE /HARDWARE **COPYRIGHTING & PATENTING**

DISTRIBUTED AND OBJECT ORIENTED DATABASES

MYTHS & REALITIES IN HIGH PERFORMANCE COMPUTING

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Monday, February 29, 9 AM - 5 PM (one per day only)

1. ☐ SOFTWARE REUSE
2. ☐ VHDL
3. ☐ COMPUTER ARCHITECTURE
4. ☐ SOFTWARE QUALITY CONTROL

Friday, March 4, 9 AM - 5 PM (one per day only)

5. ☐ NEURAL NETWORKS
6. ☐ MICROCHANNEL
7. ☐ FAULT TOLERANT

(note: program subject to change)

Requests for refunds must be received in writing no later than Feb. 19, 1988. Tutorial space is limited, attendance is on a first-pay, first-serve basis. Conference registration fee includes one copy of the *Compcon Digest of Papers*, as well as admittance to the conference hosted party.

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Payment should be sum of boxes checked. No purchase orders.
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Credit card registration is available by phone.

Tutorials – Monday, 29 February 1988 – 9:00 am to 5:00 pm – luncheon included

Software Reuse Update

Instructor: Will Tracz, IBM

Audience: Those with an interest in new or advanced ideas on developing software systems to enhance programmed productivity and product quality by reusing programs, porogram segments, designs, or other software artifacts.

Abstract: This tutorial will analyze the technical, political, psychological, social and economic issues related to reusing software. It will identify and analyze current software reuse approaches as they apply to several problem domains including programming-in-the-small versus programming-in-the-large and programming-at-large. Special emphasis will be placed on the separation of data from algorithm, documentation to support reuse and reusable software guidelinees.

VHDL Tutorial

Instructors: Moe Shahdad &
Kenneth Bakalar, CAD Language Systems.

Audience: This tutorial is designed for technical managers and design engineers who are familiar with a conventional high level programming languages.

Abstract: VHDL is a hardware description language for design and documentation of electronic digital systems. It may be used for system level, register transfer level, and gate level representations of digital systems. The VHDL tutorial will discuss language capabilities for describing dataflow, structure, and behaviour in VHDL. This will be followed by a discussion of techniques for representation of timing information, parametric information, and regular structutres. The tutorial will also give an overview of various VHDL tools.

Computer Architecture Choices

Instructor: Yale Patt, Univ. of Calif. Berkeley

Audience: This tutorial is particularly useful to the technical manager, engineer or OEM system designer who needs to make decisions and wants one man's quick, in depth, as much as possible survey of what is going on out there.

Abstract: It seems like the demands of the market place has resulted in every new cockeyed scheme getting implemented these days! Our job in this tutorial is not to examine why that is true, but rather to understand some of the differences, if any, in these new chips, architectures, and systems being offered. RISCs, Dataflow, new processor chips, various approaches to concurrency, multi-cubes and interconnection problems are among the issues that will be treated.

Software Quality Control

Instructor: Edward Miller,
Software Research Inc.

Abstract: This seminar surveys practical contemporary Software Quality Control (SQC) methods, identifies typical process efficiencies, and presents a number of case studies of successful SQC projects performed by the speaker's company. Modern software development processes, even including those fully supported in advanced development environments, suffer from software defect rates ranging up to 40-80 defects per 1000 lines of code (KLOC), measured over the entire software life cycle. For expert systems, which can be viewed as a special kind of software, latent defect rates can approach 100 per 1000 rules (KRULES). SQC methods are aimed at discovering a very high percentage (99.99%) of such defects. Both static and dynamic analysis approaches are used. Methods include detailed code and system inspection, hierarchical functional testing, reliable high test coverage, symbolic evaluation, and several varieties of randomized testing.

8:30 Welcome to COMPCON General Conference

Tuesday, March 1, 1988

FEATURED SESSIONS

8:30 - 9:30 **Developments in Integrated Device Technologies – MICHAEL CALLAHAN, CEO, Monolithic Memories, Inc.**

9:45 - 10:45 **Update on RISC Architectures – JOHN HENNESSY, Professor, Stanford University & Chief Scientist, MIPS Computer Systems,**

PROCESSORS

11:00 - 12:30
Alternative Implementations of the SPARC Architecture – Fred Buelow, AIDA Corp.

- *CMOS Gate Array Implementation of SPARC* – R.Chueh, L.T.Quach, Fujitsu
- *CMOS Custom Chip Implementation of SPARC* – L.Goss, Cypress Semiconductor Corp.
- *A High Performance, High Density Bipolar Implementation of SPARC* – L.Soltesz, Bipolar Integrated Technology

1:45 - 3:15
TRON Project Overview – Prof. Ken Sakamura, Univ. of Tokyo

- *An Implementation Based on BTRON Specification* – Y.Imai, M.Ando, M.Kobayashi, Y.Koshiki & K.Sakamura, Matsushita Electric
- *System Design of 32-bit Microprocessor TX3* – K.Okamoto, M.Miyata, Y.Masubuchi, H.Kishigami & T.Sato, Toshiba Semiconductor
- *A 32-bit Microprocessor Based on TRON Architecture: Design and Evaluation of TRON-CHIP GMICRO/100* – T.Shimizu, T.Yoshida, Y.Saito, M.Matsuo & T.Enomoto, Mitsubishi Electric

3:30 - 5:00
Emerging Processors – Yale Patt, UC Berkeley

- *The Architecture of the V60/V70 Microprocessor* – Y.Yano & Y.Sato, NEC Corp.
- *Architecture of the WE 32200 Chip Set* – M.Nelson, B.Ng & W.Wu, AT&T Information Systems
- *REGULUS: A High Performance CPU Chip Set* – S.Sims, J.Benkual & P.Sweere, Computer Consoles Inc.

ARTIFICIAL INTELLIGENCE

11:00 - 12:30
Recent Developments in Intelligent Machine Technology – Dr. Raymond Harrigan, Sandia National Lab.

- *Control of Robots in Hazardous Environments* – R.Harrigan, Sandia National Lab.
- *AI and Robotics* – L.Kaelbling, SRI International
- *Mobil Robots* – K.Dave, T.Linden & J.Park, Advanced Decision Systems

1:45 - 3:15
Prolog Update – Yale Patt, UC Berkeley

- *Prolog At UC Berkeley* – Prof. Despain, UC Berkeley
- *Prolog At University of Illinois* – Prof. Padua, Center for Supercomputing Research
- *Prolog at University of Oregon* – Prof.Conorey, Univ. of Oregon

3:30 - 5:00
Open Mike
Jim Warren, Silicon Gulch Gazette

Air your ideas! You have up to ten minutes to present proposals, discuss mistakes, suggest projects, report on work in progress and communicate cautions. Sign up with the Chair to air your hotly-held heresies.

HIGH PERFORMANCE COMPUTER SYSTEMS

11:00 - 12:30
Myths vs. Reality-1: Using Parallel Computers Horst D. Simon, NASA-Ames Research Center

- *Parallel Programs on the Cray and the Alliant: A Comparative Evaluation* – M.Bieterman, Boeing Computer Services
- *Massive Parallelism vs. High Speed Vectorization* – O.McBryan, Univ. of Colorado
- *Challenges in Matching Parallel Architectures and Matrix Algorithms* – R.Benner, Sandia National Lab.

1:45 - 3:15
Myths vs. Reality-2: Programming and Performance on Advanced Computer Systems Creve Maples, Sandia National Lab.

- *The Good, The Bad, and The Ugly: Comparing High Speed Computer Systems* – K.Jordan, Argonne National Lab.
- *Programming and Performance on a Cube-Connected Architecture* – G.Montry, Sandia National Lab.
- *Experience with the BBN Butterfly* – J.Mellor-Crummey, Univ. of Rochester

3:30 - 5:00
Mini-Supercomputers – Kenichi Miura, Fujitsu America, Inc.

- *Cydrome Cydra 5* – B.Rau, Cydrome Inc.
- *Sequent Symmetry Parallel Processing System* – G.Fielland, Sequent Computer Systems
- *Supertek STK-6401* – M.Fung, Supertek Computers, Inc.

STORAGE TECHNOLOGIES

11:00 - 12:30
Magnetic Storage Devices – Al Hoagland, Santa Clara Univ.

- *Capacity Gain From New Recording Head Designs* – G.Mowry, Control Data Corp.
- *Small Disk Arrays - The Emerging Approach to High Performance* – F.Kurzweil, Maxtor
- *Rotary Heads - New Directions For Tape Backup* – J.Rodriguez, Exabyte Corp.

1:45 - 3:15
Optical Storage – Dr. Geoffrey Bate, Santa Clara University

- *Technological Limits to Magnetic Recording* – G.Bate, Santa Clara Univ.
- *Error Management in Optical Disk Recording* – I.Turner, Laserdrive Ltd.
- *Systems Applications and Implications of Optical Storage* – R.Zech, Rothchild Consultants

3:30 - 5:00
Disk Caching – Dr. Jai Menon, IBM Almaden Research Center

- *The IBM 3990 Disk Cache* – M.Hartung, IBM
- *Disk Caching in the Spectrum Computer* – A.Kondoff, Hewlett-Packard
- *The Amperif Cache Disk System* – Steve Fuld, Amperif Corp.

SOFTWARE POTPOURRI

11:00 - 12:30
Object Oriented Programming – Doug Bryan, Stanford University

- *Self: The Power of Simplicity* – D.Ungar & R.Smith, Stanford Univ.
- *Objective C* – B.Cox, Productivity Products International
- *Smalltalk Program Development Environment* – G.Krasner, Park Place Systems

1:45 - 3:15
Object Oriented Databases – Dr. Daniel Fishman, Hewlett-Packard Labs.

- *An Overview of GemStone - An Object Oriented Data Manager* – M.Williams, Servio-Logic Corp.
- *An Overview of the VBASE Object-Oriented Database System* – G.Landis, Onthologic Inc.
- *An Overview of the Iris Object-Oriented DBMS* – D.Fishman, Hewlett-Packard Labs.

3:30 - 5:00
Distributed Processing Systems – Dr. Ahmed Elmagarmid, Penn State University

- *Distributed Shared Memory in a Distributed System* – B.Fleisch, UCLA
- *An Implementation Scheme for Distributed Transaction Processing* – D.Mannai & A.Elmagarmid, Penn State Univ.
- *A Paradigm and System for Design and Test of Distributed Applications* – J.Fagerstrom & L.Stromberg, Linköping University, Sweden

5:00 - 6:00 SOCIAL HOUR ON MEZZANINE

8:30 **IEEE Computer Society Awards Ceremony**

Wednesday, March 2, 1988

FEATURED SESSION

9:00 - 10:00 **Computer Market Update – GORDON BELL**

PARALLEL PROCESSING

10:30 - 12:00
Parallel Processing Systems – Ken Stevens, Jr., NASA-Ames Research Center

- *Navier-Stokes Computer* – D.Nosenchuck, Princeton Univ.
- *AMT DAP510* – D.Parkinson, Active Memory Technology
- *A Highly Parallel VAX Design Research Project in Parallel Processing* – J.Sopka & M.Reilly, Digital Equipment Corp.

SOFTWARE ENGINEERING

10:30 - 12:00
Engineering Information Systems Panel Session Prof. Mohammed Ketabchi, Santa Clara Univ.

- *Professor Gio Wiederhold*, IBM
- *Bob Winner*, IDA
- *Lt. John Ebel*, US Air Force, Wright Patterson AFB
- *Sandra Heiler*, Computer Corporation of America

WORKSTATIONS

10:30 - 12:00
SONY NEWS Workstation – Yukio Takeyari, Sony Corporation

- *System Design of NEWS Workstation* – K.Tanaka, Sony Corp.
- *Japanese Language Processing on NEWS Workstation* – K.Doi, Sony Corp.
- *CD-ROM System Based Upon NEWS Workstation* – K.Kimura, Sony Corp.

COMPUTER AIDED DESIGN

10:30 - 12:00
Update on New Standards for Hardware Design: VHDL and EDIF – Dr. Youm Huh, Stanford Univ.

- *VHDL: Language Features Revisited* – R.Waxman & J.Ayler, Univ. of Virginia
- *EDIF Version 200 an Update* – Ri.Newton, UC Berkeley
- *An Interface Between VHDL and EDIF* – M.Shahdad, CAD Language Systems, Inc.

LEGAL ISSUES

10:30 - 12:00
Software Compatibility and Copyright Law – Dr. Robert Wedig, Wedig Consulting Services

- *Recent Decisions on the scope of Copyright Protection for Software* – R.Johnston of Blanc, Gilburn, Williams, & Johnston
- *Cloning the IBM PS/2 Series–Legal and Practical Problems* – G.Davis III of Schroeder, Davis, & Orliss Inc.
- *Copyright Protection, Compatibility, and Cleanroom Process* – D.Seigel of Skjerven, Morrill, McPherson, & Friel

1:30 - 3:00

A VLSI Family For Multiprocessing Systems – John L. Payne, National Semiconductor

- *The NS32532 Processor* – D.Schanin, National Semiconductor
- *The NS32580 Floating Point Processor* – S.Ben-Chorin, National Semiconductor
- *The NS32600 Cache Controller* – L.Quinones, National Semiconductor

3:30 - 5:00

A New Mid-Range VAX Multiprocessor System – Dileep Bhandarkar, Digital Equipment Corp.

- *Hardware System Overview* – Digital Equipment Corp.
- *Multiprocessing Software Overview* – Digital Equipment Corp.
- *System Performance* – Digital Equipment Corp.

1:30 - 3:00

Software Reuseability – Will Tracz, Stanford University

- *SEI Software Reuse Project* – R.Holibaugh, Carnegie-Mellon Univ.
- *IDeA: Reuse Project* – C.Richter, MCC
- *SPC Reuse Project* – B.Barnes, Software Productivity Consortium

3:30 - 5:00

The Use of Integrated Project Support Environments, IPSE, for Large-Scale Software Development – Dr. Ram Banin, Atherton Technology

- Market Impact of Software Development Environments – A.Rappaport, The Technology Research Group
- Requirement for Tool Integration into an IPSE – B.Boehm, TRW-DSG
- Issues in CASE Tool Integration – A.Wasserman, IDE
- Architecture of an Integration and Portability Platform – W.Paseman, Atherton Technology
- Trends in Software Development Environments for Large Software Systems – R.Ellison, Carnegie-Mellon Univ.

1:30 - 3:00

Sun Microsystems SPARC Architecture – Dave Ditzel, Sun Microsystems

- *The Scalable Processor Architecture (SPARC) and a CMOS Gate Array Implementation* – R.Garner, A.Agrawal & M.Namjoo, Sun Microsystems
- *Compiler Technology for SPARC* – S.Muchnick & A.Wu, Sun Microsystems
- *Unix on SPARC* – S.Kleiman, Sun Microsystems

3:30 - 5:00

The New Apollo Workstations Environment – Paul Levine, Apollo Computer Inc.

- *The Network Computing System: An Environment for Developing Distributed Applications* – T.Dineen, P.Leach, N.Mishkin, G.Wyant & J.Pato, Apollo Computer Inc.
- *The Cache Architecture of the Domain Series 4000* – C.Frink & P.Roy, Apollo Computer Inc.
- *A Portable, Extensible Environment for Developing Interactive Applications* – K.Hinckley & A.Schulert, Apollo Computer Inc.

1:30 - 3:00

Advances in the VHDL Design Environment – Dr. Youm Huh, Stanford Univ.

- *A State of the Art VHDL Simulator* – D.Coelho & A.Stanculescu, Vantage Analysis Systems, Inc.
- *VHDL in an Object Oriented Design Environment* – M.Chung, E.Rogers & Y.Won, Michigan State Univ.
- *A VHDL Synthesis System* – S.Krolikoski, Honeywell Inc.

3:30 - 5:00

Standards and Benchmark Circuits in Digital-Testing – Prof. Samiha Mourad, Santa Clara Univ.

- *Benchmark Circuits for Digital Testing* – P.Goel, Gateway Design Automation Corp.
- *IEEE Standard Logic Symbols: Why Use Them?* – F.Mann, Texas Instruments
- *EDIF Test Generation and Fault Simulation* – J.Eurich, Engineering DataXpress, Inc.

1:30 - 3:00

Patent Protection for the Computer Industry – Dr. Robert Wedig, Wedig Consulting Services

- *The Patent/Copyright Interface for Software Protection:Determining the Proper Role of Each* – R.Laurie of Townsend & Townsend
- *Why You Should Listen When Your Patent Attorney Calls* – D.Simo of Spensely, Horne, Gubis, & Lubitz
- *Legal Issues Panel of the Speakers*

3:30 - 5:00

Open Mike

Jim Warren, Silicon Gulch Gazette

Air your ideas! You have up to ten minutes to present proposals, discuss mistakes, suggest projects, report on work in progress and communicate cautions. Sign up with the Chair to air your hotly-held heresies

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Thursday, March 3, 1988

FEATURED SESSIONS

8:30 - 9:30 **Developments in Neural Networks – FEDERICO FAGGIN, President, Synaptics**

9:45 - 10:45 **Emerging Workstation Platforms**

NEURAL NETWORKS

11:00 - 12:30

Introduction to Neural Networks – Fred Coury, Fred Coury Associates

- *Introduction to Biological Nervous Systems* – C.Clanton, Consultant
- *Introduction to Neuron Models* – P.Ransil, Lockheed AI Center
- *Introduction Neural Network Models* – M.Jurik, ESL

1:45 - 3:15

Implementations of Neural Networks – Fred Coury, Fred Coury Associates

- *Neurosymbolic Learning for Prallel Graphics Stream Generation* – P.Bierre, Stanford Univ.
- *VLSI Implementations of Retinal Models* – M.Sivilotti, California Institute of Technology
- *Implementing a Thinking Robot* – M.Johnson & R.Scanlon, Watervliet Arsenal

3:30 - 5:00

Perspectives on Neural Networks Panel Session Fred Coury, Fred Coury Associates

- *Peter Berke*, UCLA
- *Dr. Karl Pribram*, Stanford University
- *Dr. Stuart Dreyfus*, UC Berkeley
- *Tom Schwartz*, Tom Schwartz Associates

DATABASES

11:00 - 12:30

High Performance Relational Database Systems – Jim Gray, Tandem

- *Non Stop SQL - A Distributed Relational DBMS* – R.Holbrook, Tandem
- *Informix Turbo* – D.Curtis, Informix
- *Measure of Work Station DB Performance* R.Catell, SUN Microsystems

1:45 - 3:15

High Performance Transaction Processing Systems: Case Studies – Andreas Reuter, Institut fur Informatik, Stuttgart

- *Disaster Recovery* – J.Lyon, Tandem
- *The Mead Information Retrieval System* – S.DeFazio, Mead Data Central
- *Camelot-A Transaction Processing System for the UNIX environment* – A.Spector, Carniege Mellon Univ.

3:30 - 5:00

Distributed Databases Bahram Mahbod, HP Laboratories

- *Site Autonomy in a Distributed Database Environment* – R.Cornelis, Sybase, Inc.
- *Approaches to Distributed Database Management* – J.Baker, Oracle Corp.
- *to be announced*

HIGH END SCIENTIFIC WORKSTATIONS

11:00 - 12:30

The Dana Personal Supercomputer

- *Complete Cray-Class, 2-chip Vector Unit* – G.Miranker, Dana Computers
- *Cache Coherence in Multiprocessor Vector Architectures* – J.Robenstein, Dana Computers
- *High Speed Pipeline Scalar Processing via Score Boarding Techniques* – J.Sauguinetti, Dana Computers

1:45 - 3:15

The Advent of the Personal Supercomputer Workstation – Creve Maples, Sandia National Lab.

- *Steller Personal Supercomputer* – C.Methias, Steller Computers
- *Silicon Graphics Personal Supercomputer* G.Chessen
- *to be announced*

3:30 - 5:00

Integration of Symbolic, Numerical, and Graphical Techniques in Scienctific Computing Environments – Dr. S. Kamal Abdali, Tektronix, Inc.

- *Relationship Between Symbolic and Numerical Computing* – C.Moler, Dana Computers
- *Application of Numerical Computing* – G.Blankenship, Univ. of Maryland

The Graphical Interface – D.Wong, Kent State Univ.

POTPOURRI

11:00 - 12:30

Next Generation Buses – Anatol Koganivich, Signetics Corp.

- *New Advances in ECL Bus Designs* – J.West, Signetics Corp.
- *Futurebus Protocol* – P.Borrill, Spectra-Tek UK Ltd.
- *Shared Memory Systems Using Futurebus* – P.Sweazey, National Semiconductor
- *Pi-Bus Interface* – W.Ruszczyk, Texas Instruments

1:45 - 3:15

Tandem CLX Design Methodology – Theresa Fredricks, Silicon Compilers

- *A Highly Integrated Fault-tolerant Minicomputer: The Non-stop CLX* – D.Lenoxki, Tandem Computers
- *A Multi-faceted Design for Test Strategy* – D.Garcia, Tandem Computers
- *Design Methodology for System Correctness* – P.Fu, Tandem Computers

3:30 - 5:00

Computer-Aided Perception: Enhancement for Tele-Operation – Dr. Steve Ellis, NASA-Ames Research Center

- *Enhancement of Man-Machine Communication* – S.Ellis, NASA-Ames Research Center
- *VIEWS a Tele-Presence Display Environment* – S.Fisher, NASA-Ames Research Center
- *From DataGlove to DataSuit* – J.Grimaud, VPL Research
- *Image Model Control for Image Processing* L.Stark & W.Kim, UC Berkeley

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STUDENT COMPUTER BRIDGE CONTEST

Thursday, March 3, 1988

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Tutorials – Friday, 4 March 1988 – 9:00 am to 5:00 pm – luncheon included

An Introduction to Artificial Neural Networks

Instructor: Patrick Ransil, Lockheed AI Center & Mark Jurek, ESL

Audience: This tutorial is for all computer professionals, especially those with interests in parallel, adaptive or fault tolerant computing.

Abstract: This tutorial will provide a background in the fundamental principals of neural models and an understanding of their potential applications. Topics will include motivating principles from neuroscience and parallel computing, supervised and unsupervised learning rules, matching neural architectures to specific applications and a survey of current research in industry and academia.

Microchannel Interfacing

Instructor: John Figueroa,
On Target Associates

Audience: All those interested in the new IBM PS/2 Microchannel architecture and how it affects system design.

Abstract: Treats important issues concerning the new IBM PS/2 personal computer system's input/output bus.

Don't be mystified as to how the new IBM PS/2 Microchannel works any longer, this turial is for you.

This important new standard will affect personal computer design for years to come.

Fault Tolerant Distributed Software

Instructor: Ahmed K. Elmagarmid,
Penn State University

Audience: Computer Practitioners, Scientists and Technical Managers.

Abstract: This tutorial covers issues in fault tolerant distributed software.

The use of the transaction processing model in distributed operating systems and distributed database management systems will be explained in detail.

The audience will be familiarized with recovery and synchronization techniques used in distributed software. Issues in heterogeneous distributed systems software will be discussed. Case studies will be studied both from the distributed operating system and distributed database areas.

COMPCON Spring '88
Program Committee

Hasan AlKhatib, Program Chair
Santa Clara University
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Alan Bell, XEROX PARC
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Ken Muira, Fujitsu America, Inc.
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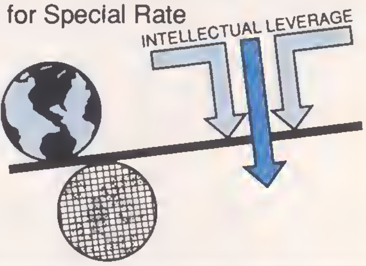

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- EMERGING PROCESSOR TECHNOLOGIES
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- PERSONAL SUPERCOMPUTERS
- MINI SUPERCOMPUTERS

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- CASE
- VHDL
- EDIF
- NEURAL NETWORKS

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- STORAGE TECHNOLOGIES

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ADVANCE PROGRAM COMPCON Spring '88, Feb 29-Mar 4!

SURVEY & TUTORIAL SERIES

An Introduction to Integrated Optics for Computing

James J. Sluss, Jr., David L. Veasey, and T. E. Batchman
University of Virginia

Edward A. Parrish, Jr., Vanderbilt University

This introductory article explores how integrated optics, taking advantage of the unique properties of photons, is creating new devices for optic signal processing and computing.

The development of integrated optics as a viable technology for applications in communications and data processing is historically linked to the fields of microwave engineering and thin-film optics. Fueled by the invention of the laser and preliminary investigations into the feasibility of low-loss optical fibers for communications, vigorous new research efforts began in the late 1960s, focusing on the fabrication of proposed integrated optical devices to create a new form of "laser circuitry".[1,2] Efforts to analyze and produce passive devices, such as low-loss dielectric and semiconductor waveguides and directional couplers, increased the understanding of how electromagnetic surface waves propagate in thin films. Investigations into the development of active devices led to advancements in semiconductor lasers, electro-optic and acousto-optic modulators, and thin-film photodetectors. Two separate approaches to the realization of integrated optical circuits were pursued: a hybrid approach, where several devices were fabricated on different substrates and subsequently bonded together, and a monolithic approach, where all devices were fabricated on a common substrate.

Initial research on integrated optical devices and circuits was stimulated because of the perceived need for compact, rugged, and economical fiber-optic repeaters which were insensitive to external thermal and mechanical variations, and immune to electromagnetic interference from surrounding electric fields. Using optical frequencies for all data transmission functions, it was predicted that significantly higher usable bandwidths could be achieved. High reliability and small size would be attainable through application of batch fabrication technology. All of these advantages clearly defined the great potential of integrated optics.

Since these early experimental attempts at integration of optical devices for data transmission, the field has evolved slowly, finding a few niche applications in higher speed data processing. Today, optically simple but functionally complex circuits are being manufactured for signal processing applications. These circuits usually offer the system designer a compact, economical, high-bandwidth device for Fourier transform and correlation operations that would normally require complex electronic circuits ranging in size from several circuit boards to mainframe computers. The one-dimensional nature of these devices is appropriate for high-speed spectrum analysis of communication and radar data streams.

With this brief history on integrated optics as background, some of the fundamentals of integrated optics will be discussed so that the subsequent articles may be better understood. This discussion will include both guided wave optics and free space optics. While the primary concern is not with free space optics, a cursory coverage of lenses is necessary because many of the fundamental operations are the same as in guided wave optics, and certain systems that have been proposed make use of both guided and free space optics.

The properties of the photon are fundamental to this discussion. Its speed is limited by the material in which it travels. The implication of this is that optical computing speed is ultimately limited to the velocity of light in the material, ($c = c_o/n$), which may be on the order of 1.5 x

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10^{10} centimeters per second for $n = 2$. The time delay for a photon traveling 1.5 cm is thus 0.1 nanoseconds.

The second important property of photons is that they may or may not interfere depending on the coherence properties (phase relationship) of the photons in the individual beams. Two light beams can intersect in free space or in a dielectric waveguide with no interference occurring while, at the same time, photons from coherent sources will interfere constructively or destructively when combined after traveling different paths. Both of these properties are advantageous in optical computing and signal processing devices. In contrast, electrons interact with each other through their electric fields and repel or attract other charged particles.

A third fundamental property of the photon used extensively in optical devices is that the energy of the photon is related to its frequency through Planck's constant ($E = h\nu$). This energy for the photon is generated through the transition of an electron or molecule between energy states in a material which has been excited. Thus, the frequency of the photon can be selected by choosing the proper material (e.g., semiconductor materials).

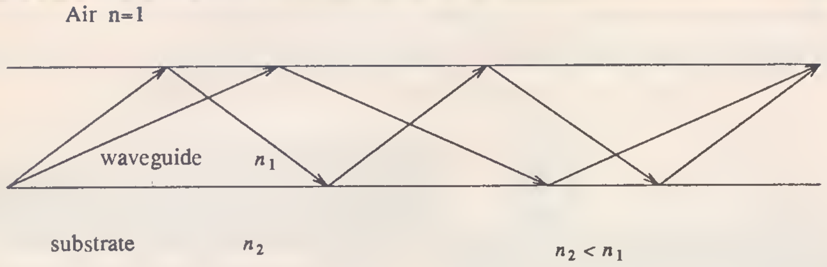

Figure 1. Ray trace approximation of two modes in a thin film waveguide.

Transmission of information via photons requires no conducting materials but relies solely on low-loss dielectrics or free space. Over short distances (< 1 meter), the bandwidth of either the optical waveguide or the free space path is limited only by optical modulator technology, whereas the bandwidth of an electronic system is limited by the inductance and capacitance of the metallic transmission path. Although this bandwidth advantage may be exciting, one has to pay the price of larger individual device dimensions. Waveguide dimensions will be on the order of an optical wavelength (1 micron), and most devices are a factor of 10 or more larger. Meaningful size and speed comparisons between electronic circuits and integrated optical circuits must be made on the basis of functional operations (i.e., correlation, convolution, etc.) rather than on individual circuit elements. The speed and parallelism of the optical components may lead to a smaller packaged circuit even though individual devices are larger than submicron VLSI devices.

Finally, the photon can be refracted by a lens or diffracted by a slit or pinhole. It will also be scattered by impurity particles

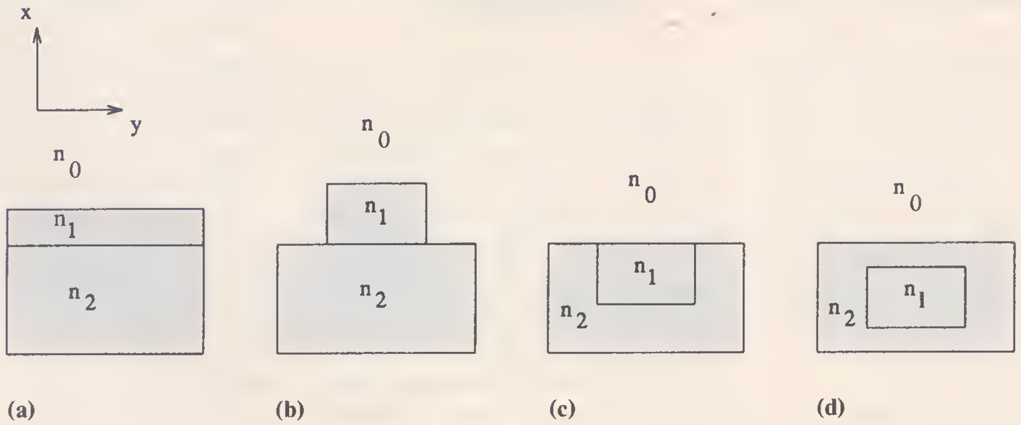

Figure 2. Thin film waveguide (a), strip loaded waveguide (b), buried channel waveguide (c), embedded channel waveguide (d).

or absorbed by a material, and it is also reflected by certain materials. The fact that some of these properties could be explained by electromagnetic wave theory, while others could not, led to the field of quantum mechanics and, in particular, quantum optics. While a detailed discussion of the properties of photons is beyond the scope of this introduction, it is sufficient to point out that photons exhibit a number of properties different from electrons and provide many new and entirely different possibilities for optical computing. Thus, photon computing should not be viewed simply as another method for duplicating existing computer architectures and operations but should be looked upon as a unique technology with new potential for computing.

Optical waveguides

Integrated optical circuits rely on the guiding of electromagnetic energy at optical frequencies (10^{14} - 10^{15} Hz) in waveguides. Here, laser beams are restricted to a thin sheet of light propagating through the waveguide. The basic principle behind the guiding of lightwaves is Snell's law (see "Reflection and refraction" on page 17), which defines the incidence angles at which a ray of light in a dense medium (higher refractive index) will be totally internally reflected at the boundary with a medium which is less optically dense (lower refractive index). If the region where total internal reflection occurs is bounded on either side by less optically dense materials, the light ray will be confined to the more dense material and optical waveguiding will occur as illustrated in Figure 1.

With this as background, consider a few fundamental waveguiding structures which can easily be fabricated in any dielectric material. The simplest of these structures, a planar waveguide, is shown in Figure 2a with propagation in the *z*-direction. This structure confines the wave in only the *x*-direction and is considered infinite in both the positive and negative *y*-directions. Figure 3 is a photograph showing guiding in such a planar waveguide. It is a top view of the propagating wave beginning at the left where light is coupled into the guide through a prism coupler. The light propagation stops further down the guide because a thin semiconductor film has been deposited on the surface to demonstrate absorption in cladding films. Taking into account the fact that the light ray in Figure 1 may be polarized with the electric field vector in the plane of the page or perpendicular to the plane of the page, two sets of modes will exist for this waveguide: transverse electric (TE) and transverse magnetic (TM). Different angles (θ_1) represent different modes of propagation, and only certain angles are allowed because the wave must experience a 360-degree phase shift in propagating from the top refracting boundary to the bottom boundary and back again. Confinement in the *y*-direction is provided by the structures shown in Figures 2b, 2c and 2d, which introduce further complexities into the mode structure. Figure 4 shows this mode structure for a few low-order modes, where modes have been labeled according to the number of maxima in the *x*- or *y*-directions.[3]

The problem of determining how a lightwave will propagate in the more complex structures in Figure 2 soon exceeds the capabilities of ray trace analysis. As in any type of wave problem, Maxwell's equations must be solved with the proper boundary conditions to obtain the propagation characteristics of the guide (attenu-

Defining terms

Bistability: the property of having two stable output states for a given input.

Evanescent field: a nonbound decaying field.

Heterojunction: a junction formed between two dissimilar semiconductors.

Homojunction: a junction formed between two similar semiconductors.

Index of refraction: the ratio of the speed of light in a vacuum to the speed of light in the material.

Quantum well: a thin layer of smaller bandgap material sandwiched between layers of larger bandgap material; this arrangement quantum-mechanically confines the electrons in the smaller bandgap material, resulting in a substantial increase in the carrier mobility.

Speed of light: (in a vacuum) $c_o = 3\times10^8$ meters per second; the speed of light is related to the wavelength and frequency of the optical wave by the expression $c = \lambda f$.

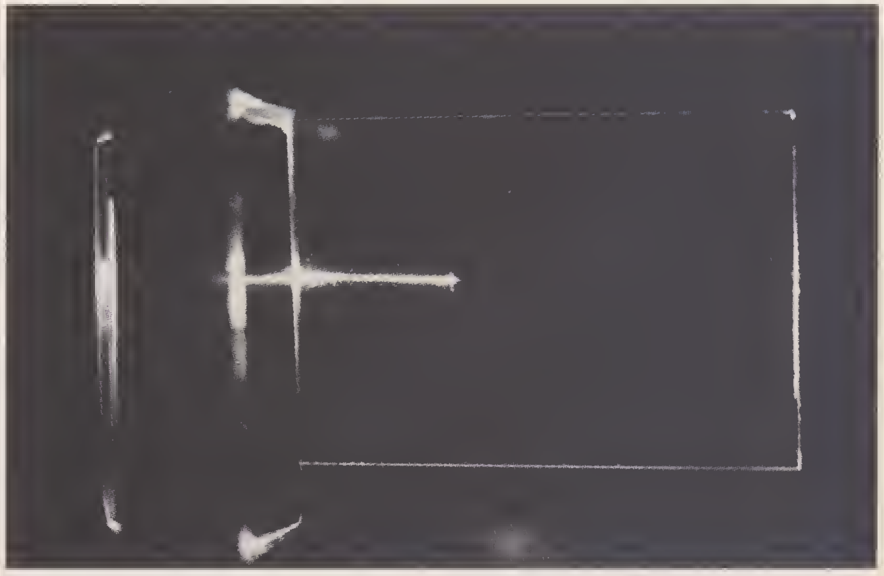

Figure 3. Guiding in planar waveguide.

ation and phase constants). For most waveguide structures, many different solutions will exist that represent individual modes of the waveguide. In some applications, it may be desirable to utilize only one or two of these modes or many of them. By proper design of the waveguide, x- and y-dimensions, and refractive indices, it is possible to select the number of modes which will propagate at a given wavelength of light λ.

The theory of waveguiding is by no means a new one. Microwave guides have been around for many years, and the analysis of such structures is a classic problem for students in electromagnetics. The optical waveguide is basically an extension of the classical microwave theory to the optical frequency region where non-absorbing dielectric materials must be used. It is important to realize that these optical waveguides are much smaller than microwave guides and, thus, hollow metal guides would be both impractical to fabricate as well as extremely lossy. The size of an optical rectangular waveguide is 5 to 10 μm by 2 μm. Obviously this is not approaching the submicron fabrication capability available in the semiconductor industry today. The limiting size of the waveguide is determined by the wavelength of light used and the dielectric constants of the materials.

It should be pointed out that optical fiber is nothing but a circular waveguide where total internal reflection occurs because the core (center region) of the fiber has a higher refractive index than the surrounding cladding. Fibers are generally fabricated from quartz glass. Because of the low loss of fibers ($<$ 1dB/km at 1.3 μm wavelength), they have been proposed for optical interconnects between VLSI chips and integrated optical devices.[4]

The waveguide that is most useful for computing and signal processing applications is the rectangular waveguide fabricated either with dielectric materials or optically active materials. Dielectric waveguides are usually fabricated by RF sputtering, ion implantation, or ion exchange on high purity quartz glass and are low loss ($<$ 1dB/cm), so that little energy is required from the source for typical propagation distances ($<$3 cm) in optical processing devices. Integrated optical waveguides are also fabricated on a number of active materials that are either semiconductor, electro-optic, or acousto-optic in nature.[4] These include lithium niobate, lithium tantalate, tantalum pentoxide, niobium pentoxide, silicon, GaAs, GaAlAs, and other III-V compound semiconductors on which active devices can be fabricated to change the amplitude or phase of the propagating lightwave.

The development of monolithic computing elements has been made possible by the ability to construct waveguide structures in active materials, such as semiconductors. Laser diodes or light emitting diode arrays, waveguides, lenses, couplers, detector arrays, and high-speed electronics can be fabricated on the same substrate using conventional semiconductor processing technology. Waveguides constructed on optically active material usually exhibit some undesirable properties such as excess losses due to absorption of optical power. Recent advances in such waveguides indicate the guiding properties of these materials can be optimized to minimize the losses over the relatively short distances required for optical circuits.[5]

Integrated optical devices

Integrated optical devices, such as lenses, modulators, laser diodes, filters, and photodetectors, can all be placed along optical waveguides. Since these devices operate on a sheet of light, they will be planar (one-dimensional) in nature (e.g., a linear detector array). These devices are divided into two major types for review in this section: passive devices and active devices. Passive devices are those that require no external energy supply for their operation such that optical signals emerging from the device are attenuated from the original entering signal level. Active devices are generally those which require some form of external energy for their operation. Passive devices can be fabricated from a variety of materials, including dielectrics and semiconductors. In contrast, active devices are dependent on some electro-optic, acousto-optic, or semiconductor material as the basis for device formation.

Passive Devices. The optical waveguide must be supplemented by several other important devices that will allow optically encoded information to be launched or intercepted and utilized. Among such passive devices are input/output couplers, directional couplers, filters, lenses, and gratings. These devices essentially provide the means to manipulate light signals in such a way that they can be used to perform computing functions. The lens is probably one of the most important devices for computation and will be covered in detail later in this article.

Optical input/output couplers are essential elements in integrated optics because they provide a means for launching light into waveguides or integrated optical circuits as well as a means for extracting optical signals. Among the different types of couplers are (Figure 5) end-fire couplers, end-butt couplers, prism couplers, grating couplers, and tapered-waveguide couplers.[5]

One of the easiest ways to launch an optical signal into a dielectric waveguide is through use of the end-fire method, which uses a lens to focus a free-space laser beam onto the end face of a waveguide. To achieve effective coupling, the field profile of the optical source must be approximately matched to the field profile of one of the modes that the waveguide will support. Laser beams usually have an approximate Gaussian profile that closely matches the field profiles for the lowest order mode in waveguiding structures. Coupling efficiencies as high as 60 percent can be achieved. End-fire coupling is normally used in the laboratory when ample space and the proper vibration isolation facilities are available. It may be necessary to use this method of coupling when a mixture of both integrated optics and discrete optical devices is used in hybrid optical computers.

End-butt coupling is another simple way to couple light into dielectric waveguides (Figure 5b). The waveguide is positioned in front of the source, so that the majority of the emitted radiation will enter the end face of the guide. This method is very sensitive to positioning of the waveguide with respect to the source in both the longitudinal and axial dimensions. Accuracy of positioning must be on the order of wavelengths, making fabrication of butt-coupled devices quite difficult. Usually, alignment to these tolerances is obtained by using piezoelectrically driven micrometer heads. Efficiencies using the butt-coupling method have approached 100 percent.

Prism couplers were important to early research in integrated optics because of the high coupling efficiencies that were attained without using the end face of the waveguide structure. High positioning accuracy is not required for planar waveguides, and coupling efficiencies of up to 80 percent are obtained with relative ease. The prism coupler is based on coupling of energy in an evanescent field (due to total internal reflection at the lower boundary) into a guided wave field in the waveguide (Figure 5c). The propagation characteristics of the horizontally travelling waves in the prism are chosen so that they match the propagation characteristics of the waveguide into which they are coupling light. Alignment of the prism becomes critical when coupling into channel waveguides.

Prisms may also be used as beam splitters (Dove prism) and for separating various wavelengths into separate beams (dispersing prism). Two-dimensional optical processing devices have been constructed mainly using prism elements.[6] When a triangular region of dielectric is deposited upon an optical waveguide, it will act as a one-dimensional prism and bend the light in the waveguide such that different frequencies are dispersed at different angles in the guide.

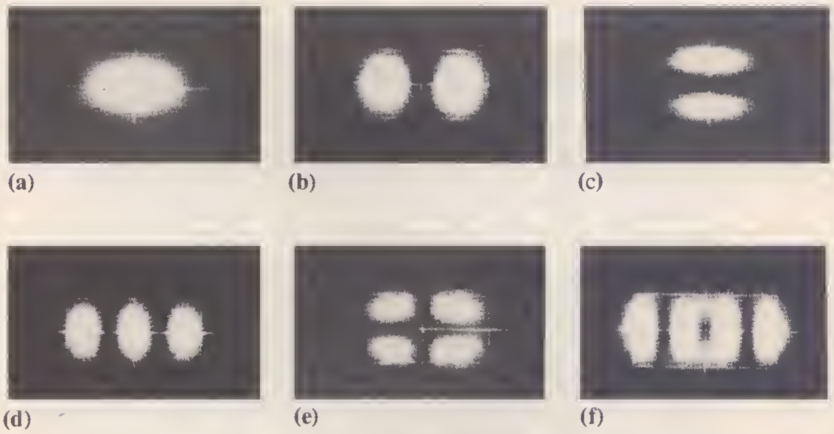

Figure 4. Modes in a rectangular dielectric waveguide: (a) E^y_{11}, (b) E^y_{21}, (c) E^y_{12}, (d) E^y_{31}, (e) E^y_{22}, (f) E^y_{41}. (Notation: E_{pq} where p is number of field maxima in x direction and q is number of field maxima in y direction.[2])

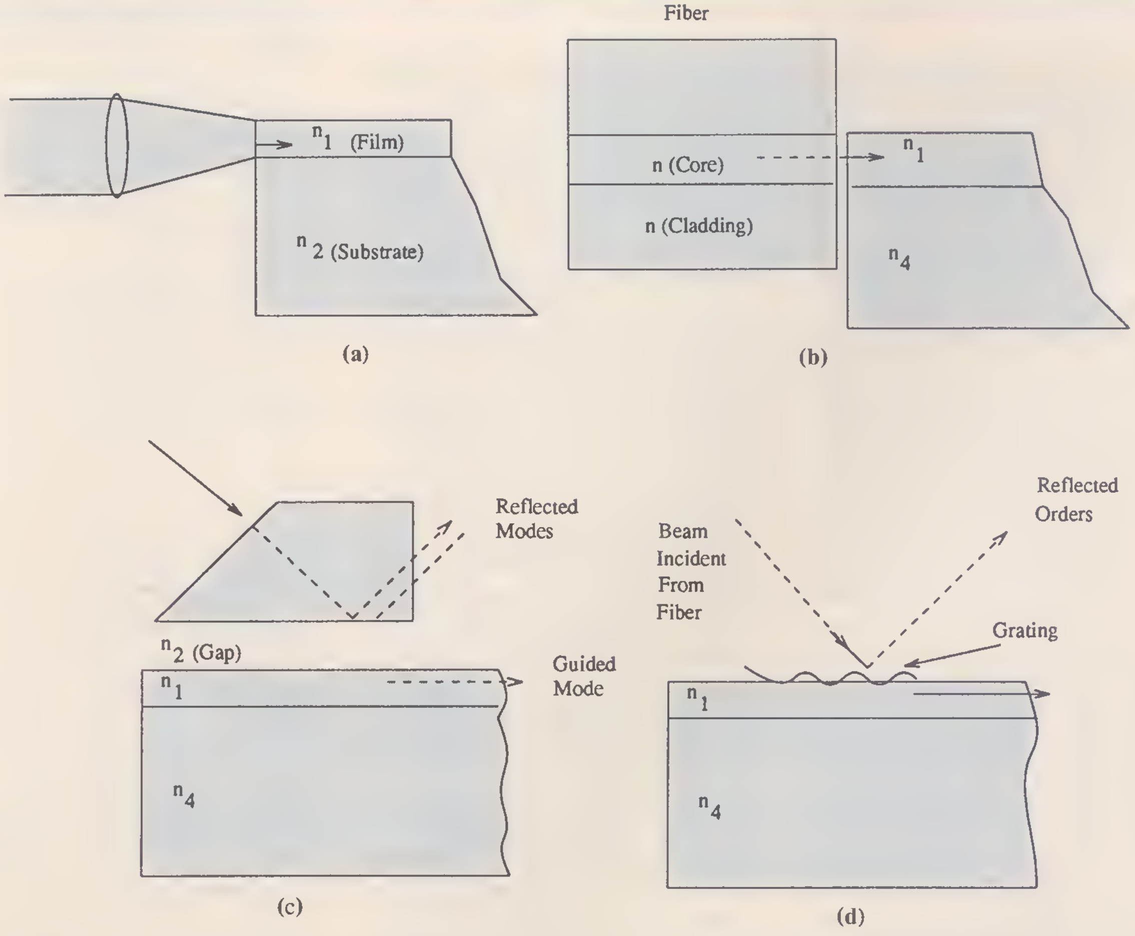

Figure 5. Waveguide coupling techniques: (a) end-fire, (b) end-butt, (c) prism, and (d) grating.

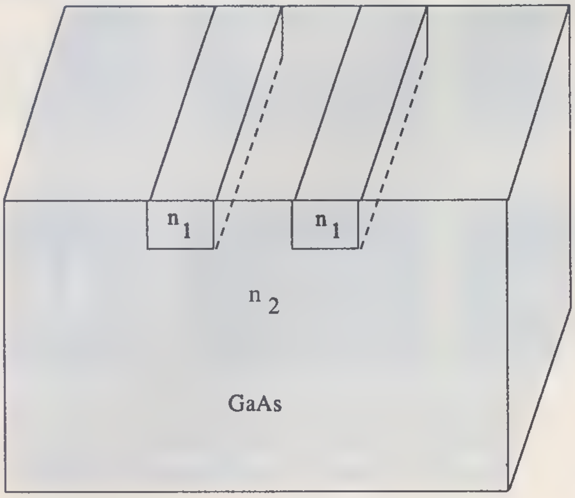

Figure 6. Dual channel directional coupler in GaAs.

Optical diffraction gratings will also function as waveguide couplers for laser beams and optical fibers (Figure 5d). Optical diffraction gratings are simply structures in which the material properties vary in some periodic fashion. Periodic modulation in materials may be in index of refraction (permittivity), in the conductivity, or in a combination of both to produce a grating on a waveguide.[7] Gratings may also be of the surface relief type on dielectric or metallic substrates where the material is machined or etched into a grating structure. Gratings operate as a coupler by diffracting an incident beam into a waveguide at or above the critical angle so that guiding can occur. Coupling efficiencies using optical diffraction gratings have reached 95 percent.[5] The main advantages of using diffraction gratings as waveguide couplers are that they can be quickly and easily fabricated on waveguides using standard semiconductor processing and that they are very compact structures. Gratings also have many other important uses relating to computation with optics. They can be used for analog-to-digital conversion, multiplexing, beam deflection and sampling, beam splitting, convolution processing, correlation processing, data processing, optical logic, data storage, filtering, image processing, and spectral analysis.[7] Gratings are also used to provide feedback in optical circuits and often replace the cavity mirrors in integrated optical lasers.

Distribution of optical energy is accomplished using integrated optical directional couplers. There are several ways to utilize directional couplers for extracting data from bus-type networks and for switching purposes. One interesting type of directional coupler is the dual-channel coupler shown in Figure 6. This type of coupler consists of two dielectric waveguides that are placed in close proximity such that the optical field profiles in the two guides overlap, causing a coupling of light between the two. Precise control of the amount of coupling may be achieved by accurate control of the interaction length between the two guides comprising the coupler. Coupling of from 10 to 100 percent can be achieved in relatively small devices. A typical 100-percent coupling device using 3-micrometer waveguides will require a coupling length of 2 millimeters.

Active devices. It is difficult to cover all the active devices that are available or are being developed for optical signal processing and computing; thus, only a few that are particularly appropriate for use in integrated optical circuits will be discussed. Many important devices, such as spatial light modulators, have been left out of this discussion because they are available only as discrete devices designed primarily for operations on two-dimensional input signals.

Sources. Most of the early research in optical signal processing used visible wavelength gas lasers as the source of coherent radiation. There were a number of reasons for this, including availability, ease of alignment, and the fact that demonstrations were impressive with red or green light. Because of the size, integration, and stability constraints imposed by optical circuits, semiconductor lasers were better suited for utilization in integrated optical systems. For those interested in the historical development of semiconductor lasers, several review papers written by pioneering investigators were featured in a recent special issue of the *IEEE Journal of Quantum Electronics*.[8]

It is useful to review some of the important properties of the semiconductor laser that have made it the light source of choice for integrated optical systems. Narrow spectral emission linewidths may be achieved, allowing accurate wavelength selectivity. The output power is sufficiently high to permit use in optical data transmission systems. The laser is a coherent light source, both spatially and temporally, resulting in an output beam that is highly directional. The dimensional characteristics of the device are such that it is compatible with both optical fibers and planar waveguides and, thus, suitable for various hybrid optical systems. With regard to monolithic integrated optical systems, semiconductor lasers may be fabricated directly on a common substrate with other active and passive integrated optical devices. The output of the laser may be accurately controlled by directly modulating the input current of the device. In this manner, amplitude, pulse, and frequency modulation may all be achieved. Other direct modulation schemes exist, making the device flexible in terms of optical computing applications. (For a description of how lasing, or the stimulated emission of photons, occurs in semiconductor lasers, see "Laser emission in semiconductors" on page 22.)

The first homojunction semiconductor lasers suffered from low efficiencies due, in large part, to their inability to achieve a high degree of optical confinement. The heterostructure laser established a means of producing better confinement of photons by introducing a waveguiding region within the laser. The use of heterojunc-

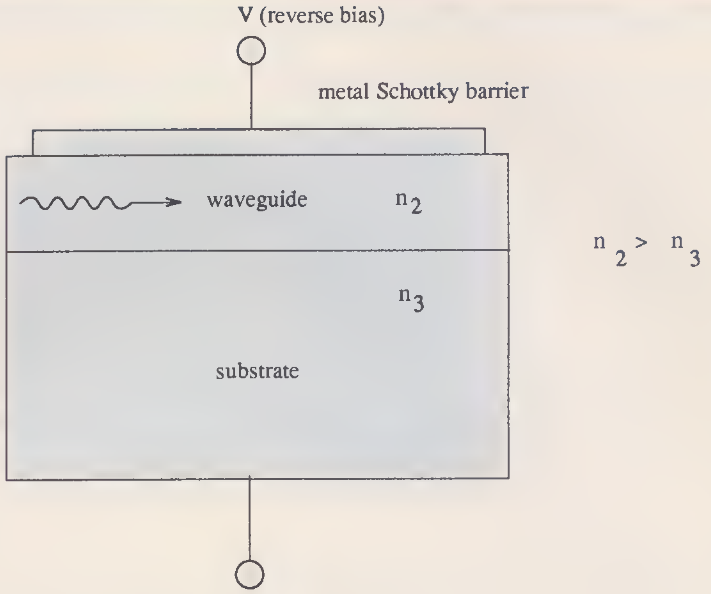

Figure 7. Single-waveguide electro-optic modulator.

tions also increased the carrier injection efficiency at the *p-n* junction. The result was the construction of semiconductor lasers that exhibited greatly reduced threshold current densities and correspondingly increased efficiencies, thereby significantly outperforming their homojunction counterparts. Further investigations led to the development of the double heterostructure laser and the distributed feedback laser. Each of these structures increased the performance levels of semiconductor lasers even further. Recently, much excitement has been generated by the report of a laser structure demonstrating threshold currents of less than 1 milliampere.[9] These graded-index separate-confinement single quantum well buried heterostructure lasers have exhibited room temperature threshold currents down to 0.95 mA, with the investigators suggesting even further realizable reductions equivalent to 0.2 mA. Such ultralow-threshold semiconductor lasers could easily be driven by TTL level signals.

The fabrication of semiconductor lasers employs many of the same processing techniques used for producing other types of semiconductor devices. Epitaxial growth techniques capable of producing monolayers of materials, such as VPE, MOCVD, and MBE* are used extensively, especially for more recent laser structures that incorporate single or multiple quantum wells into their design. Nearly all semiconductor lasers are made from GaAs and its numerous ternary and quaternary compounds. Fortunately, these materials and fabrication techniques are the same as used in high-speed GaAs digital electronics and many other integrated optical devices that allow the complete integration of electronic and optical devices onto a monolithic chip.

Modulators and switches. Electro-optic modulators are useful active integrated optical devices that are particularly well-suited for optical-signal processing applications. Operating as modulators, the devices may be used to temporally vary the propagation characteristics (amplitude or phase) of an optical carrier wave, thereby impressing information upon it. These devices may also be used as optical switches, which can either turn optical signals on or off, or reroute them by changing their spatial positions within an integrated optical circuit. One advantage such optical devices have over their electronic counterparts is a much wider usable bandwidth. Bandwidths of up to a few gigahertz have been demonstrated in some experimental devices.

The operation of electro-optic modulators is based on application of the electro-optic effect. Certain crystalline materials exhibit a change in refractive index when an electric field is applied along preferred directions relative to the crystal axes. This anisotropy comprises both linear and nonlinear components. The linear effect, commonly referred to as the Pockels effect, is most pronounced and is of primary importance in the fabrication of electro-optic modulators. The nonlinear effect, commonly referred to as the Kerr effect, is less useful in electro-optic modulators, particularly since it produces unwanted distortion of the optical signal.

A typical single-waveguide electro-optic modulator is illustrated in Figure 7. Such a device is capable of modulating both the phase and the polarization of an optical wave, although it is rather difficult to detect these types of modulations. For this reason, modulation of the intensity is most practical. Other types of electro-optic modulators are dual-channel waveguide and Bragg-effect electro-optic modulators.[5] Common materials used in fabricating integrated optical electro-optic modulators are GaAs, GaP, $LiNbO_3$, and $LiTaO_3$. In addition to their small size and amenability with well-developed fabrication techniques, integrated optical electro-optic modulators require far less power for effective operation than their bulk counterparts.

Active directional couplers (switches) involve architectures similar to the dual-channel directional couplers discussed previously, except that they make use of the electro-optic effect so that the percentage of coupled light between waveguides can be varied according to which operation is to be performed. Basically, the only difference in the construction of such devices is that they are fabricated on an electrically active material, and metal strips are placed on the surface of both parallel waveguides, with a ground plane located on the bottom of the substrate. Electric fields can then be applied across these strips to vary the refractive index of the active material in the waveguides. If this variation is precisely controlled, arbitrary coupling between the two guides can be achieved.

Acousto-optic modulators also serve as devices for optical switching and signal modulation. The primary difference is the means by which changes in the index of refraction of the waveguiding region of the device are produced. Surface acoustic waves traveling in certain crystalline materials produce mechanical strain that, in turn, induces variations in the index of refraction. This variation, known as the photoelastic effect, is periodic and has the same frequency as the acoustic waves that produce it. An effective diffraction grating is thus formed and may be used as a means of changing the direction of propagation of light waves traveling in the waveguiding region of the device.

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*VPE-vapor phase epitaxy, MOCVD-metalorganic chemical vapor deposition, MBE-molecular beam epitaxy. All are methods of depositing thin films.

The most commonly used acousto-optic modulator is the Bragg-type modulator. This device operates on the basis of the Bragg diffraction regime, where the guided light wave is oriented such that it is incident upon the induced grating region at the Bragg angle. The Bragg angle (θ_B) is given by

$$\sin\theta_B = \frac{\lambda}{2\Lambda}$$

where λ is the wavelength of the light and Λ is the grating spacing, or acoustic, wavelength. The output light is then diffracted with maximum efficiency at an angle equal to twice the Bragg angle with respect to the input. A representative Bragg-type modulator is shown in Figure 8. Like electro-optic modulators, integrated optical acousto-optic modulators require significantly less power than their bulk counterparts.

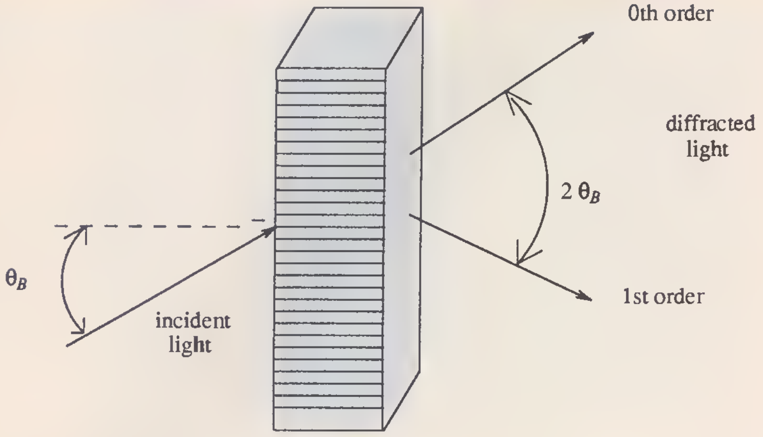


Figure 8. Bragg-type acousto-optic modulator.

Photodetectors. These are an integral part of any optical information processing scheme. Discrete photodetectors have been in use for some time, but investigations into new types of integrated optical photodetectors have tended to take a back seat to vigorous efforts into the development of new semiconductor laser structures. For integrated optical circuit applications, photodetectors with high quantum efficiencies are required so that high sensitivity can be achieved. Fast response time is a requisite characteristic, as is low power consumption.

Most commercially available photodetectors are of the depletion layer type, consisting of a reverse-biased *p-n* junction. Charge carriers produced upon absorption of incident photons within the depletion region modulate the reverse current of the diode, allowing detection of optical signals. Depletion layer devices may be fabricated directly onto semiconductor waveguides, as shown in Figure 9. The depletion region actually extends into the waveguide, thus enhancing the absorption

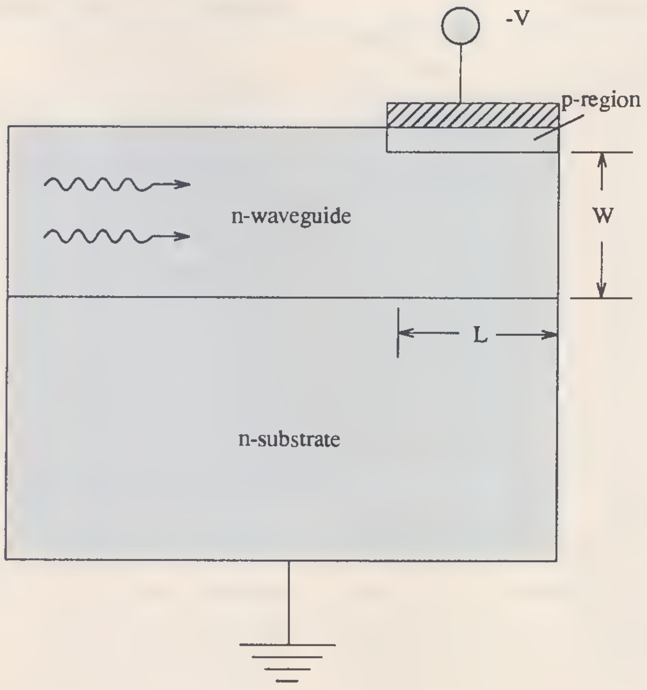


Figure 9. Waveguide photodetector with depletion width *W* and diffusion length *L*.

of photons. Consequently, these waveguide photodetectors exhibit high quantum efficiencies. If the *p*-type region shown in Figure 9 is replaced by a layer of metal, a rectifying barrier contact is formed. This type of photodiode is known as a Schottky-barrier diode and is most often used in integrated optics applications. The primary reason for the popularity of the Schottky-barrier photodiode is the ease with which it may be fabricated directly upon the surface of a waveguide.

Avalanche photodiodes are another type of useful detector for integrated optics. They offer higher gain than either depletion layer or Schottky-barrier devices and are useful when operating at high frequencies. The main drawbacks of avalanche photodiodes have been problems related to reliability, stemming from high fabrication-induced stresses.

Recent investigations have led to the fabrication of working photodetectors made from hydrogenated amorphous silicon (a-Si:H).[10] These Schottky-barrier photodiodes were formed directly on dielectric waveguides and exhibited very fast response times (on the order of picoseconds), due to favorable characteristics of the a-Si:H. These devices are important in that they demonstrate how different active and passive materials may be combined to form new hybrid-integrated optical devices without sacrificing compactness and mechanical stability.

Bistable devices. The achievement of low-power all-optical bistability in small semiconductor devices in the late 1970s led to an upsurge of interest in digital optical computers.[11] Optical bistable devices are capable of performing the optically controlled memory and switching operations necessary for many computer and signal processing applications. Most research in this area has centered on individual devices or two-dimensional arrays of such devices. Recently, interest in nonlinear guided wave phenomena has led to the demonstration of a number of guided wave devices suitable for use as integrated optical components. For optical data processing, the bistable device should be of micron or submicron size, have picosecond switching speeds, and have very low switching power requirements ($< 10^{-15}$J). This device should also operate at room temperature and at a convenient wavelength such as 1.3 μm. No devices currently exist that meet all these requirements, but there are several promising concepts that

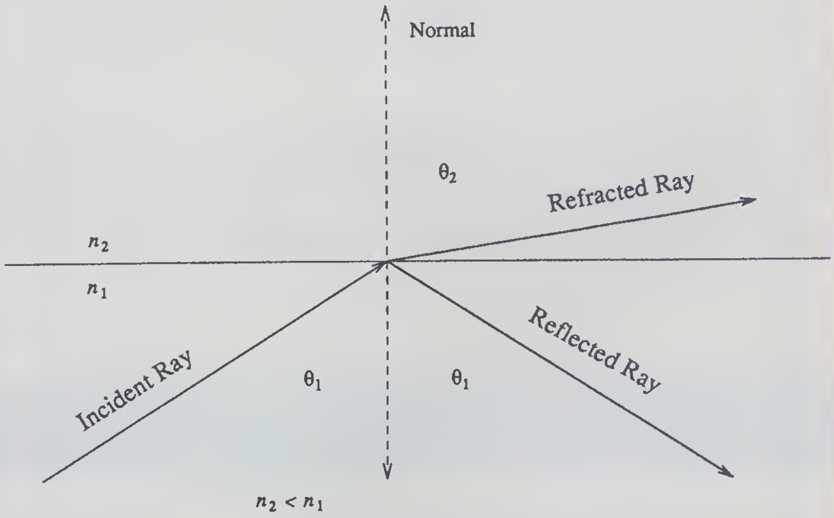
Reflection and refraction

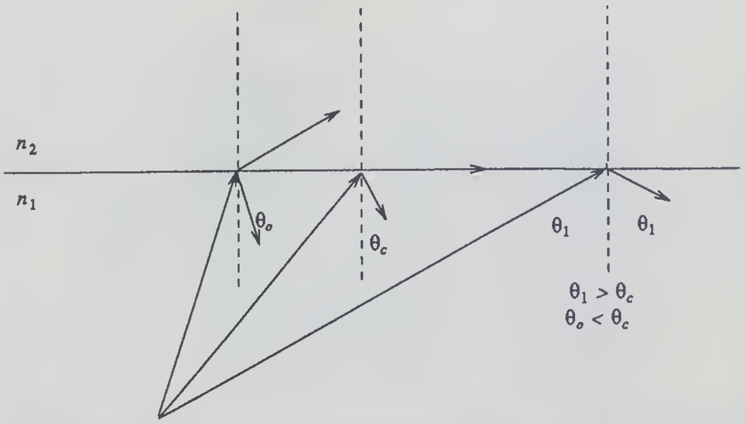
Two of the fundamental laws of optics are the law of reflection and Snell's law. Consider a light ray associated with a plane wave travelling in a dielectric material n_1 (incident ray) incident at an angle of θ_1 with respect to the normal at the interface between the two media, n_1 and n_2. When this ray encounters the boundary separating the two different dielectrics, part of the ray is reflected (reflected ray) at the same angle θ_1 (reflection law), and the remainder is bent (refracted ray) as it enters medium 2 as shown in the figure below. The relationship between the incident and refracted angles is given by Snell's law

$$n_1 \sin\theta_1 = n_2 \sin\theta_2$$

where n_1 and n_2 are the refractive indices of the two media.

As the incidence ray angle (θ_1) approaches the critical angle (θ_c), the refracted angle (θ_2) approaches 90 degrees. For larger incidence angles, no refraction is possible and the light rays are *totally internally reflected* as shown in the figure at bottom.





may prove to be practical for computing systems.

Any optical device that possesses two different steady-state transmission states for the same input intensity is considered a bistable device. Figure 10 shows the general characteristics of an optical bistable device. One of the earliest and simplest bistable optical devices was the Fabry-Perot cavity filled with sodium vapor. The Fabry-Perot cavity, or etalon, shown in Figure 11 consists of two mirrors aligned in parallel and maintained at a stable and accurate spacing. A Fabry-Perot cavity transmits the incident light when the optical length of the cavity is an integral multiple of half-wavelengths. The optical length between the two can be controlled by insertion of an optical material with a dielectric constant that is optically or electrically variable. If the volume between the two partially reflective mirrors contains an optically nonlinear material, the transmitted light intensity will follow a hysteresis curve as shown in Figure 10.

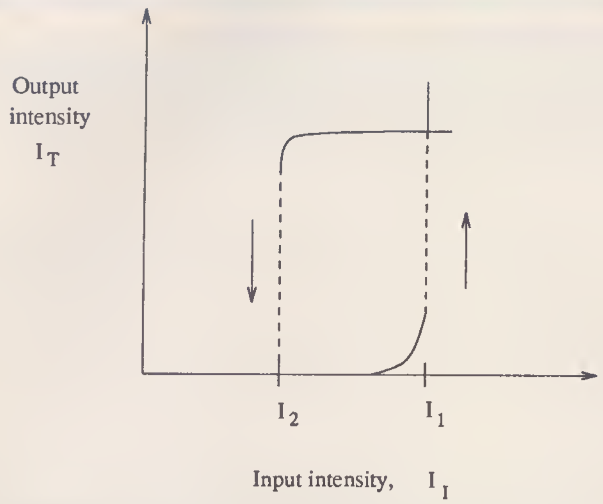


Figure 10. Characteristic curve for an optical bistable system.

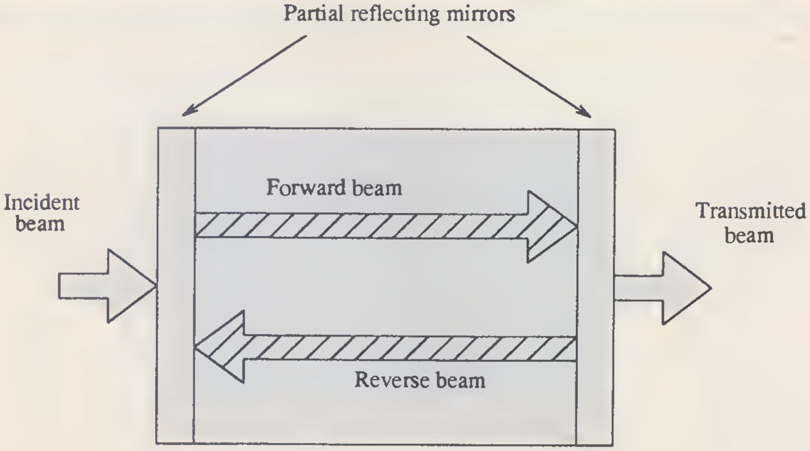


Figure 11. Fabry-Perot cavity.

When such a device is fabricated in integrated optical form, the mirrors may be replaced by gratings on a waveguide and the section of waveguide between the two gratings would contain a nonlinear optical material. This nonlinear material may also be placed on the surface of the waveguide and could be a multiquantum-well material that exhibits more pronounced nonlinear effects than those obtained using conventional semiconductors.

Fourier optical devices

The lens is a passive element and is one of the most fundamental and important devices associated with many conventional two-dimensional optical signal processing techniques. Some of the more important characteristics of the lens are discussed here, and then applications in integrated optical circuits are illustrated. First, consider a complex function g of two independent spatial variables x and y. This function may be a film transparency or any two-dimensional light variation. Suppose that a film transparency is used which has a series of vertical dark lines (no transmittance) and clear lines (complete transmittance) across the film in the x-direction so that there are f_x lines per millimeter across the film. In this particular case, $g(x,y) = g(x)$. The Fourier transform of $g(x)$ is simply

$$FT\left\{g(x)\right\} = \int_{-\infty}^{\infty} g(x)\exp[-j2\pi f_x x]dx$$

This is a spatial Fourier transform where f_x is called the spatial frequency. Now, if the transparency has both vertical and horizontal lines and the Fourier transform is taken of $g(x,y)$ then

$$FT\left\{g(x,y)\right\} =$$

$$\int_{-\infty}^{\infty}\int_{-\infty}^{\infty} g(x,y)\exp[-j2\pi(f_x x+f_y y)]dxdy$$

is the two-dimensional transform with f_x and f_y being the two spatial frequencies.[12] It can easily be shown that, if this transparent film is placed in front of a conventional two-dimensional lens at a distance, d_o, and illuminated with parallel light at the back focal plane, the amplitude distribution of the light will be the two-dimensional Fourier transform of the input transparency (Figure 12).

Not only is the lens performing a two-dimensional Fourier transform on the image, it is also operating on each point simultaneously so that a parallel computation is completed in the time it takes the lightwave to travel from the image to the lens focal plane. This parallel processing of an analog signal occurs without having to electronically quantize and convert the signal into binary form. These inherent advantages make optical processing ideally suited for many image processing applications. The ability to take two-dimensional Fourier transforms at the speed of light is fundamental to a number of other optical processing functions. For example, filtering in the frequency domain can be accomplished easily by placing a mask at the back focal plane of the lens in Figure 12. After having performed a filtering operation, a second lens may be placed at a focal length in back of this filter and result in a reconstructed, filtered image of the original transparency (Figure 13). Convolution and correlation are also relatively straightforward operations with combinations of lenses and transparencies or modulators.

One-dimensional lenses can be used in integrated optical devices since the guided wave is essentially a sheet of light. It has been demonstrated that such lenses may be fabricated on an integrated optical waveguide. Several types of integrated optical lenses have been fabricated and reported.[13] Such a lens behaves as a cylindrical lens and performs a one-dimensional Fourier transform. Figure 14 shows an example of a planar system for performing the convolution between two transparencies, $t_1(-x)$ and $t_2(x)$. It should be noted that these operations are usually much simpler if the light source is single frequency (monochromatic).

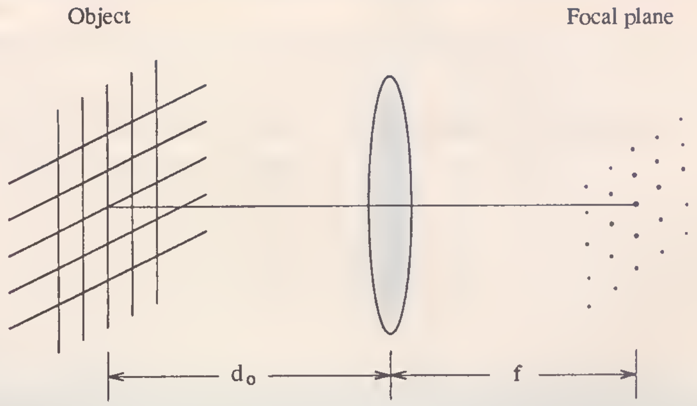


Figure 12. Fourier transform properties of the lens.

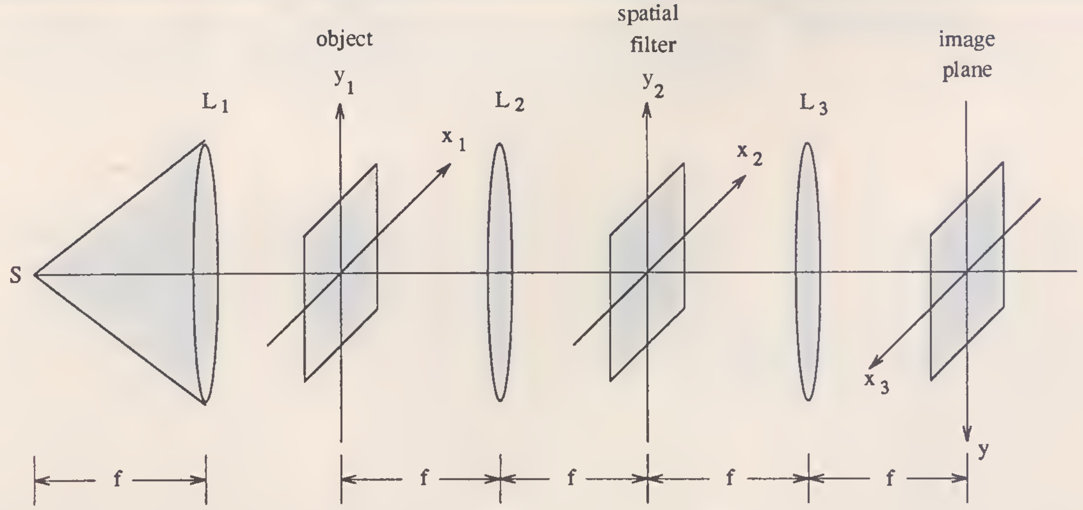


Figure 13. A configuration for coherent processing.

The integrated optical RF spectrum analyzer[5] pictured in Figure 15 and the

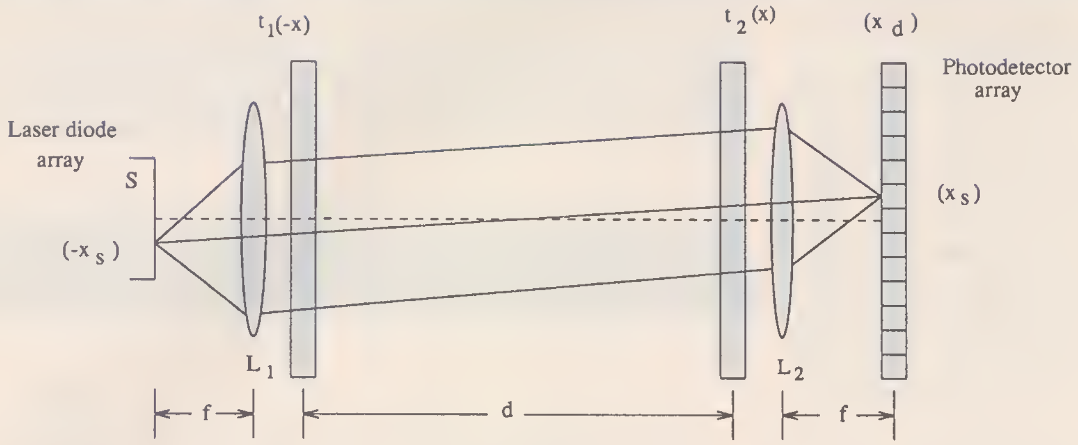


Figure 14. A lens system for performing convolution in an integrated optical processor.

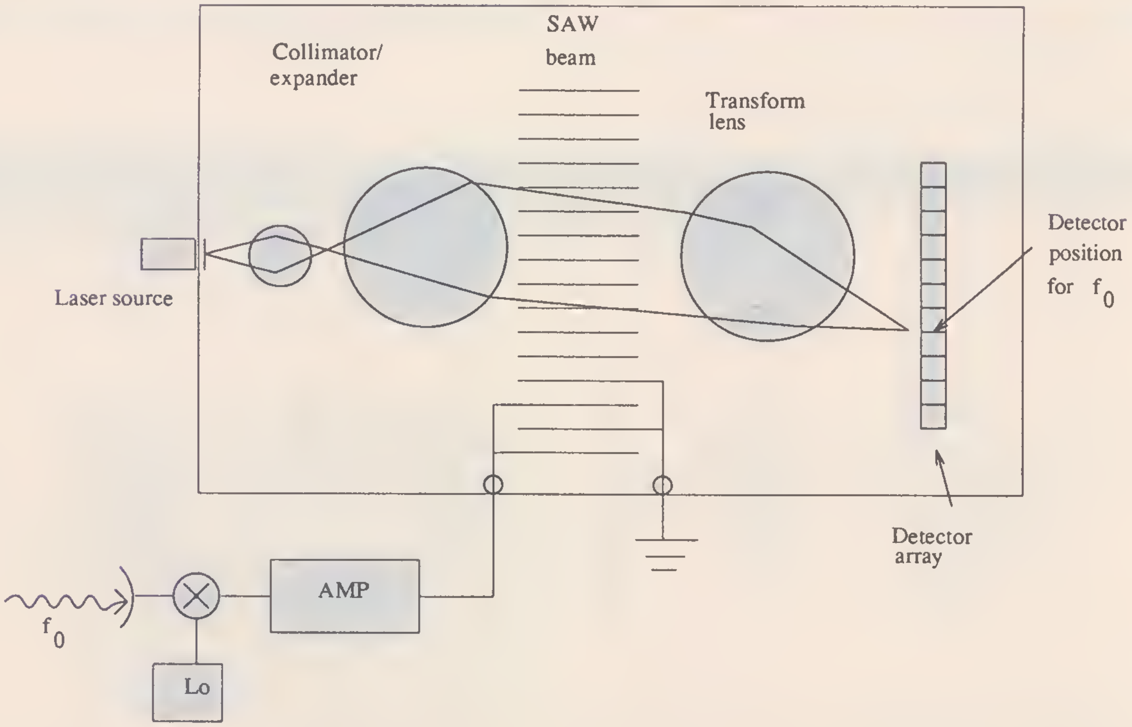


Figure 15. Integrated optical RF spectrum analyzer.

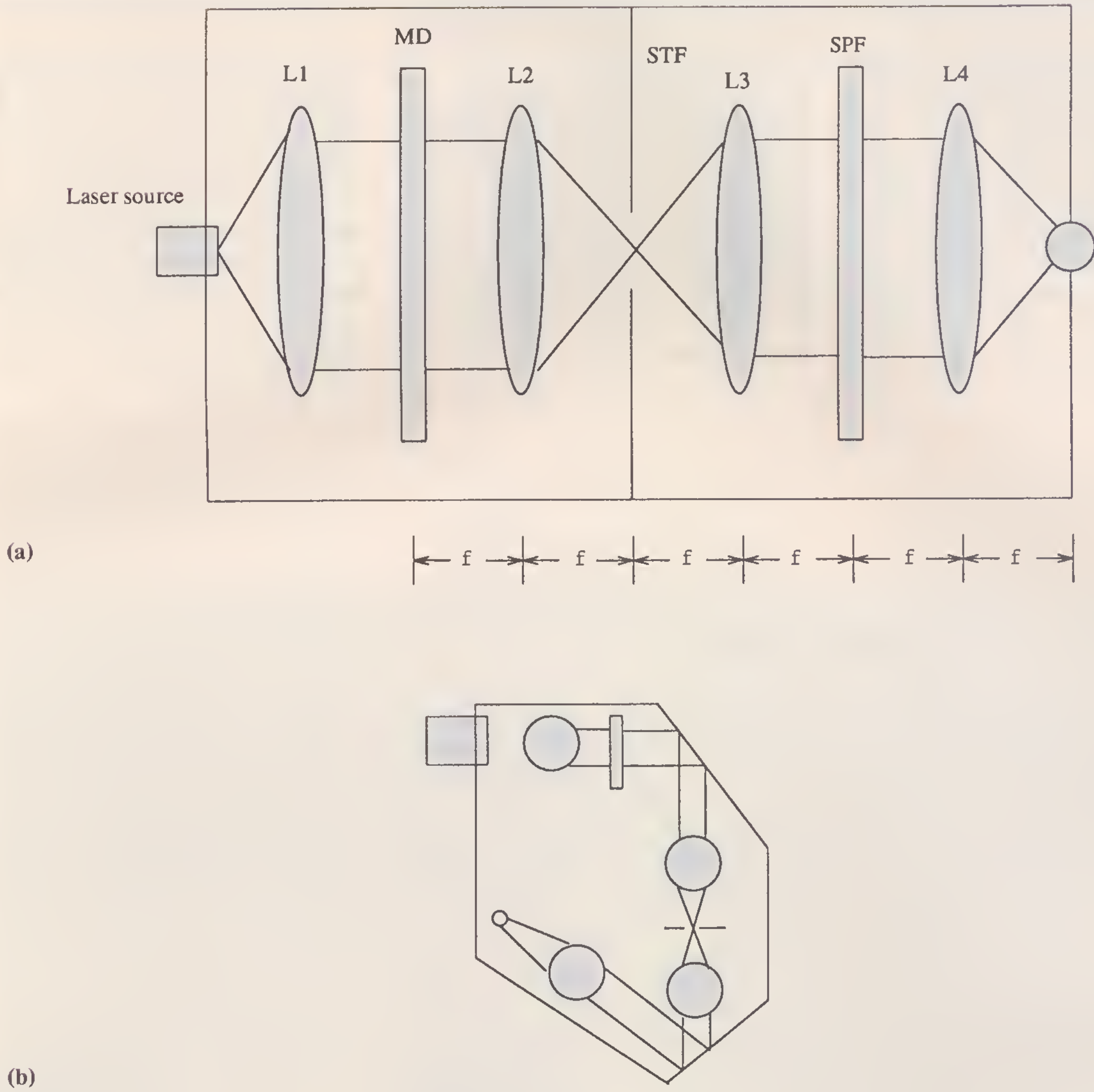


Figure 16. Integrated optical correlators: (a) linear correlator; (b) folded correlator.

integrated optical correlator shown in Figure 16 were among the first useful circuits utilized for computing. Both of these devices feature a laser diode that is butt-coupled to a planar dielectric waveguide. The waveguides have collimating lenses either deposited or machined so that they are diffraction-limited. In the spectrum analyzer, the collimated light exiting the lens encounters an optical diffraction grating that is acoustically produced by incoming radar signals. Obviously, the incoming signal contains a certain range of frequency values and has a specific frequency signature, depending on the type of radar. The acoustically generated grating diffracts light to a second lens that Fourier transforms the optical signal produced by the grating at a detector array where the lens focal plane is located. By observing the spatial distribution of the light on the detector array with prior knowledge of how the grating diffracts for different frequencies, the spectrum of the incoming radar signal can be ascertained instantaneously. This acousto-optic spectrum analyzer is ideal for use in military aircraft where it is necessary to determine whether a plane is being tracked by a ground station or any type of air-to-air or ground-to-air missile. A 500-MHz signal bandwidth can be instantaneously channelized by an integrated acousto-optic spectrum analyzer into 25-MHz bands. This yields an effective processing rate of 10^9 samples per second, more than two orders of magnitude faster than that currently available using digital signal-processing technology.

The light exiting the collimating lens L1 in the integrated correlator first encounters a modulator cell (MD) and then a Fourier transform lens L2 (Figure 16). The Fourier transform is formed at the focal plane of L2 where the spatial filter (SPF) cell is placed . The filtered signal passes through another Fourier transform lens L3 and finally encounters a detector array. The output of this device gives a measure of the correlation between the object modulator cell and the spatial filter, which can be either a mask or another modulator cell.

Regular two-dimensional lenses may also be used in combination with integrated optical circuits to form a hybrid system. One such system has been proposed by Lohmann[14] where a series of integrated optical circuits is stacked in front of a lens to form a two-dimensional data array and then a similar stacking operation behind the lens operates on the transform performed by the lens.

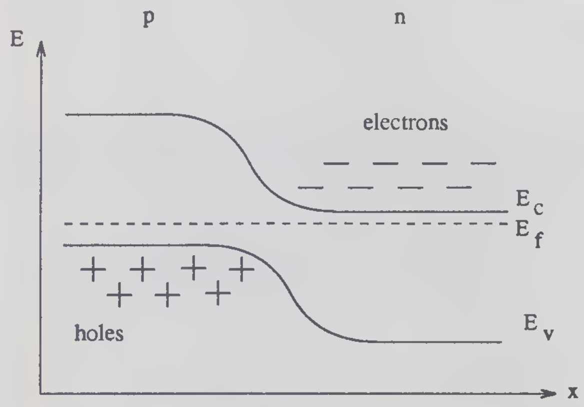
We will touch on one additional topic before concluding this discussion of lenses, and that is holographic elements. Holography is a lensless imaging process that allows one to store information on both the amplitude and phase of an incident wave from an object. With both amplitude and phase being stored, a three-dimensional image of the object is produced upon reconstruction. Phase and amplitude information is stored in a hologram through the use of interfering reference and object beams. The interference pattern generated and recorded (the hologram) must then be illuminated with the reference beam to view the information. Bulk information storage techniques using holography have been proposed and studied.

Holograms also can be used for filter functions in optical processing systems for removing aberrations and other image distortions. It has been demonstrated that holograms can be formed in optical waveguides for data processing.[15] Unfortunately, there is no simple technology for

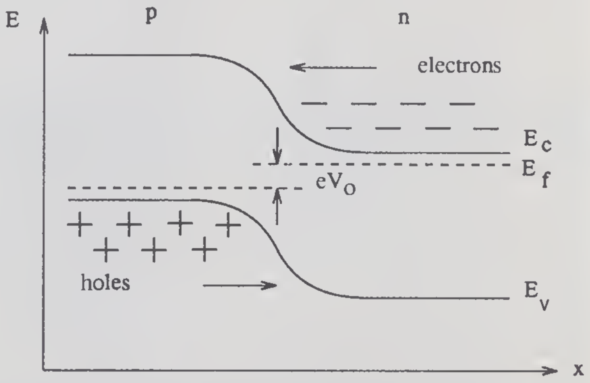
Laser emission in semiconductors

When a *p-n* junction with an energy band diagram as shown below left is unbiased, the excess holes in the valence band of the *p*-type material cannot recombine with the excess electrons in the conduction band of *n*-type material. However, when a forward bias is applied across the junction, the energy barrier separating the excess holes and electrons is reduced, as shown below right, allowing them to recombine in the depletion region. When the holes and electrons recombine, they may give up their excess energy in the form of photons. This process is known as spontaneous emission and is the principle upon which basic light emitting diodes work. If a spontaneously emitted photon collides with an electron that has not yet recombined, it may induce recombination, yielding the release of a photon that is of the same energy (frequency) and travels in the same direction. This radiative process is known as stimulated emission. Except under special conditions, the occurrence of stimulated emission is less probable than spontaneous emission.

Semiconductor laser structures must be designed so that these special conditions exist, allowing stimulated emission to predominate over spontaneous emission. The number of electrons at the bottom of the conduction band that are available for recombination with holes in the valence band must be artificially increased and maintained. The increased concentration of electrons is known as a population inversion and is accomplished by supplying an external pumping current to the laser. The minimum pumping current necessary to maintain stimulated emission is defined by the threshold current density. An intense field of photons with the proper energy to induce the emission of duplicate photons is also required for stimulated emission to predominate over spontaneous emission. This photon flux is established by forming a resonant cavity that provides sufficient optical confinement of photons within the depletion region. By maintaining a sufficient population inversion and photon flux, successful laser operation may be achieved.



A *p-n* junction light emitter with no applied bias.



A *p-n* junction light emitter with forward bias applied.

writing and erasing holograms in optical waveguides, but such a technique may become available sometime in the future.

The field of integrated optics is still not a mature technology. Remember, the transistor was invented in 1947, and integrated circuits were developed some 20 years later. Undoubtedly, there will be many new developments in integrated optics over the next few years that will impact the optical computing field and, most assuredly, optical computing will play an important role in the computer field over the next decade. Integrated optics offers the possibility of integrating all the optical components onto a common substrate in such a way that a compact, reliable, and economical computer can be developed. But this will only likely happen after systems have been constructed and demonstrated using discrete or hybrid devices.

The field of integrated optics is in a state of flux associated with the natural scientific evolution process; thus, "integrated optics" has different meanings to individual researchers. It may be a GaAs circuit containing high-speed transistors, laser diodes, and optical waveguides, or it may be a lithium niobate circuit with waveguides, couplers, lenses, and acousto-optic modulators. At this time, no one material has proven to be the material of choice, in contrast to silicon that was the material of choice in early integrated electronic circuits. Before integrated optics can become a mature technology for optical computing, additional research will be required. ☐

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T. E. Batchman and **Edward A. Parrish, Jr.**, are guest editors of this edition of *Computer*. Their photographs and biographical sketches appear at the conclusion of the article entitled "Guest Editors' Introduction: Integrated Optical Computing."

Readers may write to Batchman at the Electrical Engineering Dept., University of Virginia, Charlottesville, VA 22901.

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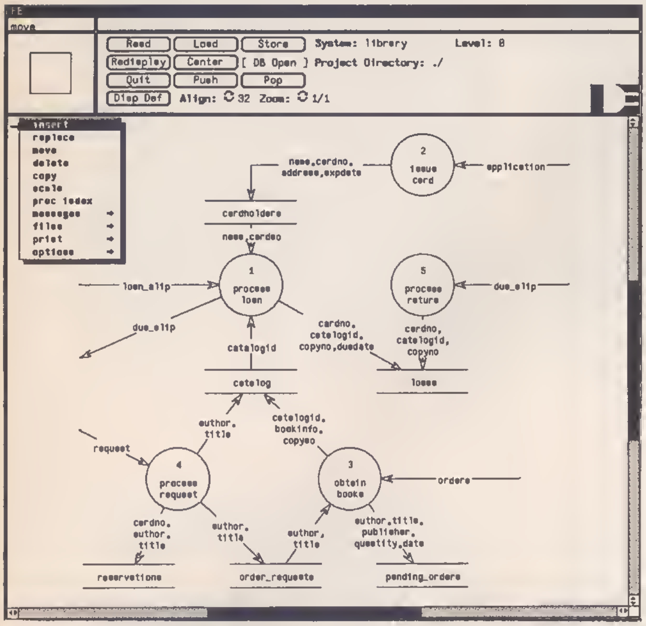

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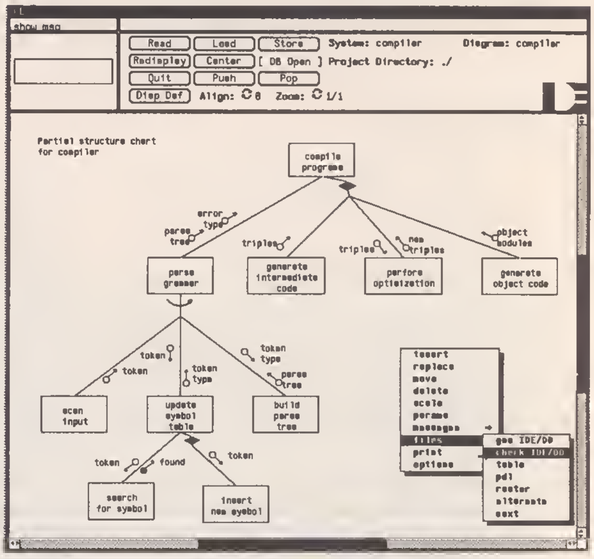

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Survey of Silicon-Based Integrated Optics

Dennis G. Hall
University of Rochester

"Integrated optics" refers to the application of thin-film and microfabrication technologies to the definition and development of miniature optical systems. Research efforts in this direction began on the heels of the development of the semiconductor laser and concurrently with the development of low-loss optical fibers. The early papers of Shubert and Harris[1] (1968) and Miller[2] (1969) discussed, respectively, the potential use of optical waveguides in signal processing and in "laser beam circuitry." They are usually cited as marking the beginning of integrated optics, although one could argue that earlier work by Osterberg and Smith[3,4] (1964) on image transmission through a planar optical waveguide was equally suggestive of the new field.

Many important devices demonstrated during the last two decades have used integrated optics. These include wavelength division multiplexers and demultiplexers,[5,6] spectrum analyzers,[7,8] repeaters,[9] analog-to-digital converters,[10] switches and modulators,[11,12] and optical digital correlators.[13] In addition, interest is growing in nonlinear integrated optics, an attempt to exploit optical nonlinearities in optical waveguide structures.[14,15]

Combining silicon and optics technologies might benefit many future applications. This article reviews past accomplishments and future possibilities for silicon-based integrated optics.

One interesting feature of all this work concerns the basic materials used. Unlike the world of electronics, which for the most part concentrates on silicon, research and development in integrated optics involve an increasing number of materials. Principal among these are lithium niobate ($LiNbO_3$) and III-V semiconductors such as gallium arsenide (GaAs).

$LiNbO_3$ is of interest for two reasons. First, it possesses a comparatively large Pockel's (linear electro-optic) effect, which allows some variation of the refractive index by means of an applied electric field. Second, it is relatively easy to form a surface optical waveguide by diffusing a small amount of titanium into a single crystal of $LiNbO_3$. GaAs is a direct bandgap semiconductor, which means that its intrinsic electronic band structure readily lends itself to the fabrication of light emitters and detectors as well as conventional electronic components. Materials such as zinc oxide, zinc sulfide, semiconductor-doped glass, certain organic materials, ferroelectric crystals, and a host of others attract interest by virtue of some special property each exhibits. This diverse materials situation for optoelectronic devices in general has led one author to comment that the optics community has not yet decided on an "optical silicon," a unique material with properties that can be exploited in a broad range of applications.[16]

Despite being the backbone of the microelectronics industry, silicon has played a relatively minor role in the development of integrated optics primarily because of two facts. First, the silicon crystal structure (diamond lattice) is centrosymmetric, therefore silicon does not exhibit Pockel's effect. Second, silicon is an indirect bandgap semiconductor, which

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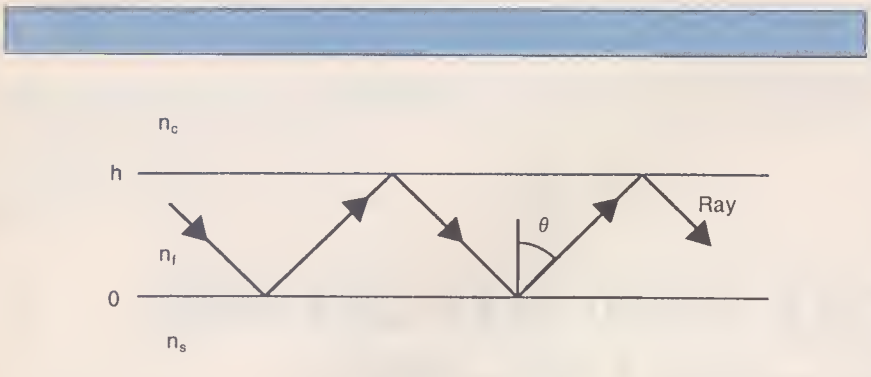

Figure 1. Sketch illustrates a light ray trapped by total internal reflection (TIR) within a layer of thickness h and refractive index n_f bounded by media of refractive indices n_c and n_s.

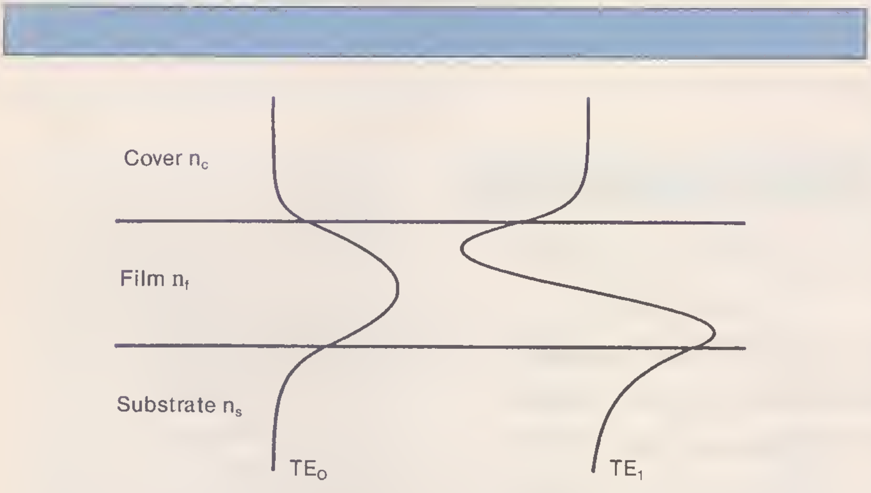

Figure 2. Plots of the electric field distribution for transverse electric (TE) guided waves with mode integers $m = 0$ (TE_0) and $m = 1$ (TE_1).

precludes the occurrence of direct, radiative, band-to-band, electron-hole recombination—the very mechanism responsible for optical emission from light-emitting diodes and diode lasers made from direct-bandgap semiconductors like GaAs. This does not mean that silicon has been ignored by the integrated optics community. In spite of the two apparent deficiencies just mentioned, the idea that one might take advantage of a mature silicon technology to combine optical and electronic components on a single silicon substrate remains a captivating one.

This idea received something of a boost when the fiber optics industry shifted its attention from the wavelength range 0.8 to 0.9 micrometers to the wavelength range 1.3 to 1.6 micrometers. Silicon strongly absorbs electromagnetic radiation in the former wavelength interval, but is transparent in the latter, which means that one can fabricate silicon optical waveguides for use at the longer wavelengths. Silicon-based integrated optics, or optoelectronics, might find a place in computing, in interconnection technology, in signal processing, in communications, or in new applications yet to emerge.

The basic idea

The central idea in integrated optics is to process and manipulate light while it is trapped within the confines of an optical waveguide. Figure 1 illustrates the ray-optics view of light trapped within a thin layer by total internal reflection. The optical waveguide consists of a layer of refractive index n_f bounded above and below by cover and substrate media of refractive indices n_c and n_s, respectively. For a sufficiently large layer thickness h and wavelength λ, there exists a discrete set of angles θ_m for which the ray is trapped, provided that the condition $n_c < n_f > n_s$ is fulfilled.

The integer m is referred to as the *mode integer*. An analysis, based on Maxwell's equations, of propagation in optical waveguides reveals that each value of m corresponds to a distinct electric field distribution and propagation constant, or phase velocity, in the waveguide. Figure 2 illustrates typical electric field profiles for the cases $m = 0$ and $m = 1$. Clearly, the mode integer m labels the number of zero-crossings of the field. It is also clear that the electric field penetrates beyond the physical boundaries of the waveguiding layer. We can expect this, because total internal reflection produces an "exponential tail" on the opposite side of the reflecting interface. This exponential tail plays an important role in integrated optics.

Integrated optics is usually considered a single-mode technology for a simple reason: Since each mode propagates with a different phase velocity, any component defined in or on the waveguide usually operates on each mode in a different way. For example, unless special care is taken, a waveguide lens will exhibit different focal lengths for different modes, even if all modes were excited by the same monochromatic source. Each polarization requires a minimum layer thickness to support each mode for $m > 0$. This means that we can exclude the so-called "higher order" modes simply by making the guiding layer thin enough. For typical materials and wavelengths in the visible and near-infrared regions of the spectrum, single-mode waveguides range in thickness from a few tenths of one micrometer to perhaps a few micrometers, depending on specific details.

Silicon-compatible waveguides

The earliest attempts to combine silicon technology with optical waveguide technology merely used silicon as a convenient substrate.[17] Since it is difficult to find a material with a refractive index greater than that of silicon ($n \approx 3.5$)—required by the total internal reflection condition—it is necessary to grow a layer of silicon dioxide (SiO_2), which has the much lower refractive index $n \approx 1.46$, on the silicon substrate before depositing the actual waveguiding layer. This is illustrated in Figure 3a.

To offer a specific example, a number of applications have used a layer of Corning 7059 glass deposited onto the oxidized silicon substrate by radio frequency (RF) sputtering. To use such a glass waveguide ($n \approx 1.56$) at the optical wavelength $\lambda = 0.85$ micrometers, the SiO_2 buffer layer must be approximately 1.5 micrometers thick to avoid substantial absorption by the silicon substrate of the energy in the exponential tail of the waveguide mode.

A more recent attempt to devise a silicon-compatible optical waveguide is illustrated in Figure 3b. In this scheme, a layer of polycrystalline silicon is deposited onto an oxidized silicon substrate, followed by a second layer of SiO_2. Two mechanisms cooperate to confine optical energy in the upper oxide layer. The first is total internal reflection at the SiO_2/air interface. The second is "ordinary" reflection at the SiO_2/polysilicon interface. The thicknesses of the layers are chosen so that this ordinary reflection exhibits very high reflectivity ($R = 99.96$ percent). This means that the optical wave in the upper SiO_2 layer can propagate a substantial distance (several centimeters), leaking energy into the lower layer at a very slow rate. Note that polysilicon is highly absorbing in the visible region of the spectrum, so the waveguide must be operated at near-infrared wavelengths. The device has reportedly exhibited a loss of 0.4 decibels per centimeter at the wavelength $\lambda = 1.3$ micrometers.[18]

We know that the presence of free carriers reduces the refractive index of a semiconductor. Figure 3c shows a silicon waveguide geometry that exploits this effect. A lightly *n*-doped layer of silicon is grown epitaxially on a heavily *n*-doped silicon substrate. Because the epitaxial layer is more lightly doped than the substrate, the epilayer can function as an optical waveguide for near-infrared (subbandgap) wavelengths for which the silicon is intrinsically nonabsorbing.

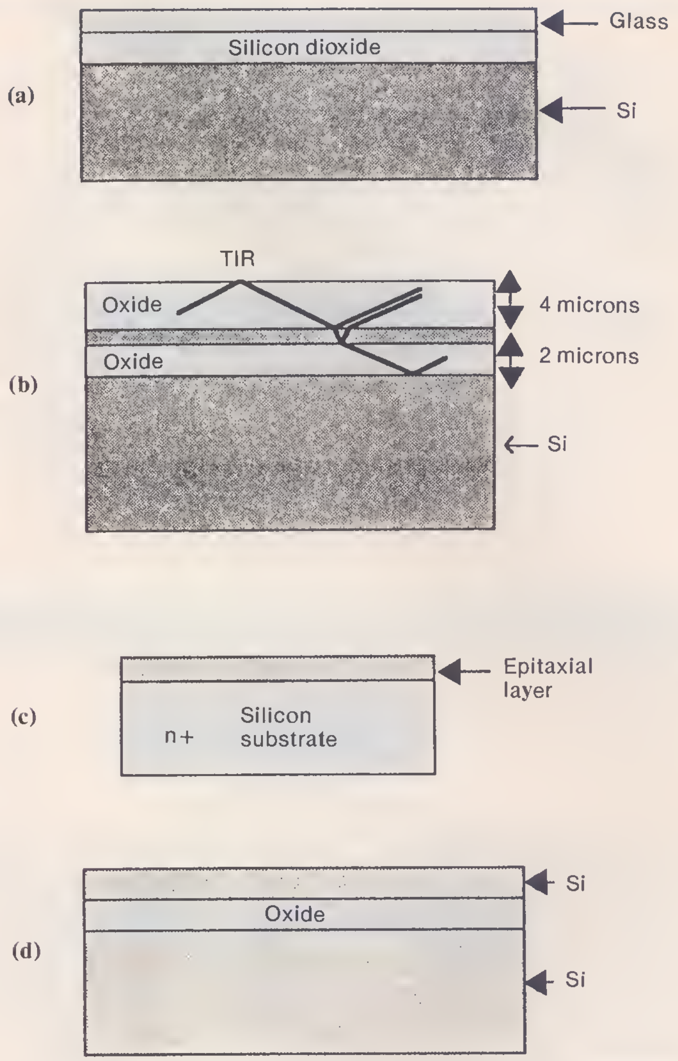

Figure 3. Four types of silicon-compatible optical waveguides: (a) glass layer deposited on oxidized silicon; (b) light confined by total internal reflection (TIR) from the topmost oxide surface and ordinary, but high, reflectivity from the bottom surface of the upper oxide layer; (c) epitaxial silicon layer formed on a more heavily doped silicon substrate; and (d) buried-oxide, silicon-on-insulator structure consisting of two crystalline silicon regions separated by a layer of silicon dioxide.

To date, this structure has been demonstrated only as a multimode waveguide, one that supports several higher-order modes in addition to the fundamental ($m = 0$) mode. One disadvantage of this epitaxial waveguide geometry is the attenuation that accompanies free-carrier absorption in the substrate. Even for subbandgap wavelengths, the exponential tail of the waveguide mode will experience strong absorption in the substrate because of indirect intraband transitions. Measurements show that this structure exhibits an attenuation of 5 to 13 decibels per centimeter at the wavelength $\lambda = 1.3$ micrometers.[19]

Figure 3d shows a promising candidate

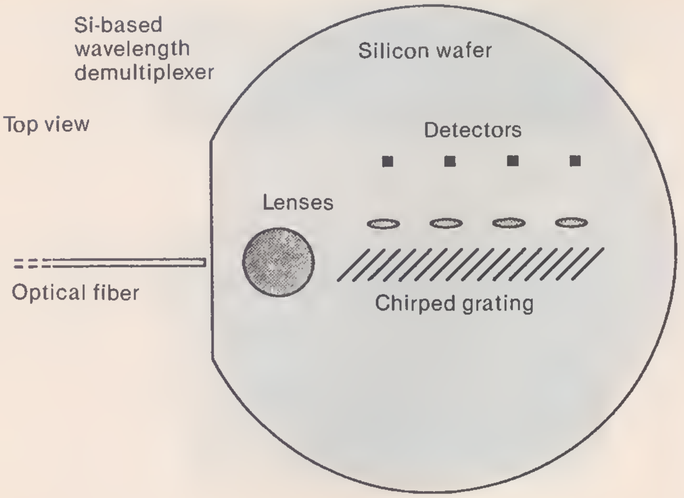

Figure 4. Sketch shows the concept for a multichannel wavelength demultiplexing system formed on a silicon substrate. The lightly shaded regions represent waveguide lenses.

for a silicon-compatible waveguide based on the so-called SIMOX (separation by implanted oxygen) technology, in which a buried oxide layer with a crystalline silicon overlayer is prepared by post-annealing a silicon wafer after oxygen ion implantation. Such wafers are being developed for radiation-hard electronics.

Recent analysis shows, however, that this very structure will also function as a low-loss, single-mode, optical waveguide for sub-bandgap optical wavelengths.[20] Operation at the wavelength $\lambda = 1.3$ micrometers with an attenuation of one decibel per centimer, for example, requires an oxide thickness of approximately 0.4 micrometers for a presumed silicon layer thickness of 0.4 micrometers. It is necessary here to isolate the silicon layer from the substrate, not because of potential absorption, but to avoid radiation leakage into the silicon substrate. Happily, only a few-tenths of one micrometer of SiO_2, a thickness readily achieved using conventional SIMOX processing, is required to achieve this isolation. It has been established that the thickness of the silicon overlayer can be increased to as much as several micrometers by epitaxial growth, so there should be no difficulty in achieving the required thickness of 0.4 micrometers.[21]

At the writing of this article, no one had yet reported demonstrating optical waveguiding in SIMOX wafers. Such experiments are underway in at least two laboratories, however, so results should appear very soon.

Integrated optical systems

Several integrated optical systems that use the silicon-based optical waveguide geometry shown in Figure 3a have been proposed and demonstrated. Discussing a few here will provide some insight about this technology.

Figure 4 shows a sketch (top view) of an integrated optical wavelength division demultiplexer developed under NASA funding by a group at McDonnell Douglas Astronautics Company in St. Louis.[6] The device was fabricated on a two-inch diameter oxidized silicon substrate coated with a layer of Corning 7059 glass, which served as a planar optical waveguide. An optical fiber mounted in a V-groove in the silicon substrate injected light into the glass waveguide through an edge (called end-fire coupling). Assume that several optical carriers, each at a slightly different optical wavelength, copropagate in the fiber. Each carrier originates from a different light source, such as a semiconductor laser, which can be modulated independently of the others. Thus, the fiber delivers several (four, in this example) information channels to the device shown in Figure 4. The actual device was configured for eight channels.

Once the optical signal enters the glass waveguide, it diverges slightly and requires collimation. This is accomplished by means of a Luneburg overlay lens, which is essentially a circularly symmetric mound, a few hundred nanometers thick at its peak, formed by depositing a high-index material like tantalum pentoxide through a mask onto the surface of the glass waveguide. The collimated guided wave then interacts with a variable period, or "chirped," waveguide diffraction grating. Such gratings are usually formed as surface corrugations (see Figure 5a) by holographically exposing a layer of photoresist deposited on the waveguide surface, developing the resist to form a mask, and then ion-milling the pattern into the waveguide.

In Figure 4, the grating lines are inclined with respect to the direction of the incident wave, and the grating period varies almost linearly along its length. This period variation causes each wavelength component of the incident wave to diffract from the original direction at a different location along the grating. Each diffracted component remains within the waveguide and is focused by another overlay lens onto its own detector, formed in the silicon substrate. Figure 5b shows a side view of a portion of the integrated optical demultiplexer to illustrate the path taken by the guided wave after leaving the grating. The McDonnell Douglas device was designed to separate spatially eight incoming channels in the wavelength interval 800 to 900 nanometers, which required a grating 19 millimeters in length.

Figure 4 is a passive system; it uses no switching or modulation elements. As mentioned earlier, silicon possesses no linear electro-optic effect, so one must look for other physical mechanisms on which to base active elements.

G.B. Brandt and collaborators, working at the Westinghouse Research Laboratories in Pittsburgh, have designed and fabricated several silicon-based integrated optical devices that use an acousto-optic interaction. The sketch in Figure 6 illus-

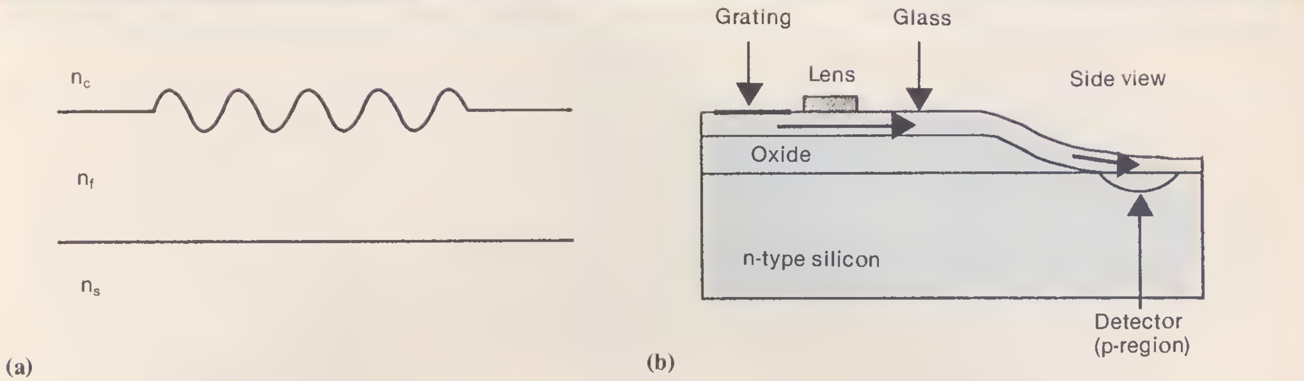

Figure 5. (a) Side view of optical waveguide with surface-corrugation grating in upper surface. (b) Side view of silicon wavelength demultiplexer. The tapered oxide directs the light guided within the glass layer to the detector region.

trates the concept for one such device, a homodyne receiver, formed on a Corning 7059 glass waveguide deposited on an oxidized silicon substrate.* The optical system is a Mach-Zehnder interferometer that employs etched silicon V-grooves as mirrors and beam splitters. One arm of the interferometer contains a zinc-oxide (ZnO) thin-film acoustic transducer. Prisms are used for input and output coupling. During operation the input optical beam, modulated at frequency ω_1, is split so that part of it interacts with the ZnO transducer, operated at the "local oscillator" frequency ω_2, in one arm of the interferometer. When the two halves of the signal are recombined at the output of the interferometer, a square-law detector mixes the signals to produce an output at the difference frequency $\omega_1 - \omega_2$, which eliminates the need for wide bandwidth detectors.

The approach common to the devices in Figures 5 and 6 appears in other devices, as well. One notable example is the RF spectrum analyzer reported by a French group in 1983.[8] The device was fabricated on a silicon nitride optical waveguide deposited on an oxidized silicon substrate. They used surface acoustic waves (SAW) launched from a ZnO transducer and deposited on the waveguide to deflect a guided optical wave through an angle determined by the SAW frequency. The deflection angle was found by using a pho-

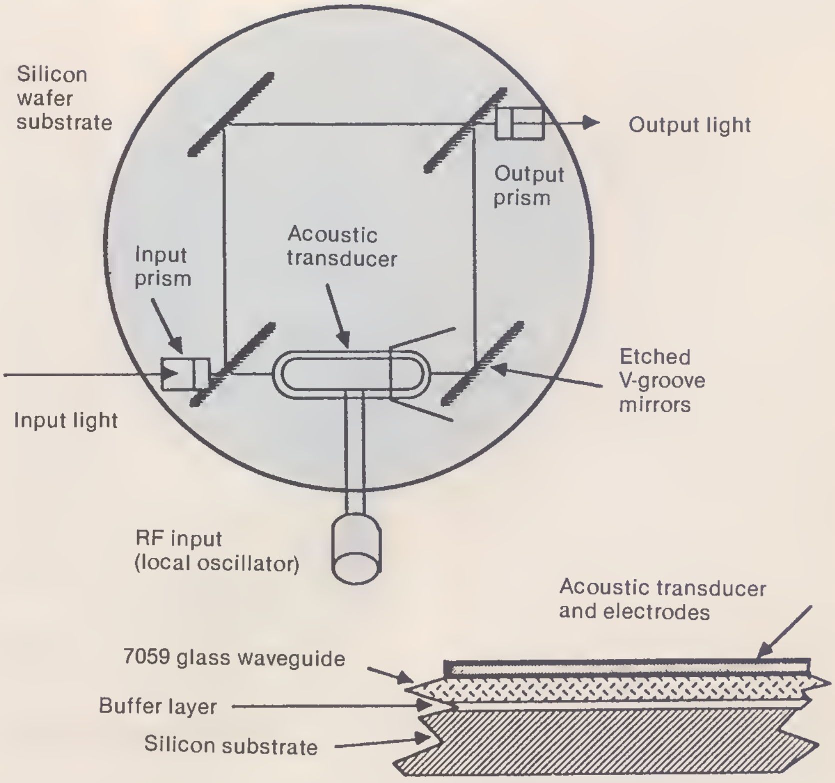

Figure 6. Sketch illustrates the basic operation of the Westinghouse homodyne receiver.

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*Funding for work on this device was provided by the United States Navy.

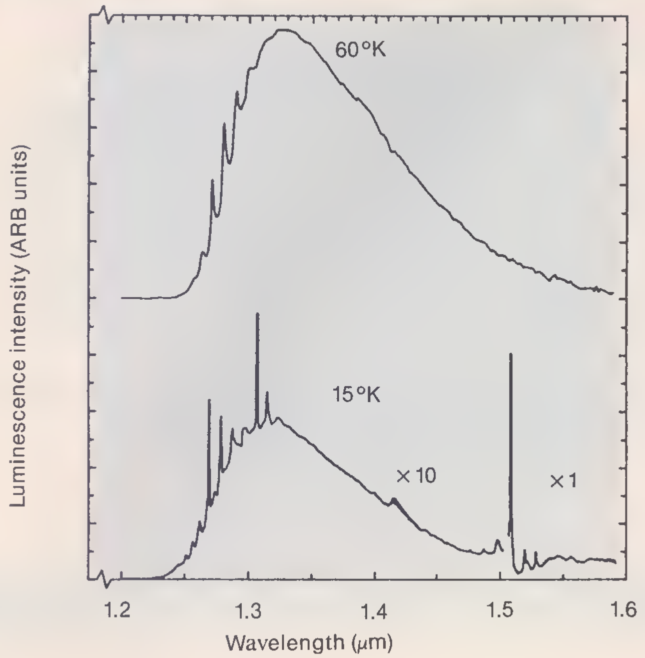

Figure 7. Spectra of optical emission from sulfur-doped crystalline silicon, at two temperatures.

todetector array to sample the location of the deflected waves at a known distance from the interaction region.

Future directions

Integrated optical devices have typically used the linear electro-optic effect for modulation and switching applications and direct, radiative, band-to-band, electron-hole recombination for optical emission. As mentioned earlier, silicon allows neither of these effects. We must find other mechanisms to provide these needed functions if silicon is to be taken seriously as a general-purpose optoelectronic material. It seems likely that silicon-on-insulator technology will provide good quality optical waveguides for optical wavelengths for which silicon is transparent. This poses a problem in itself, however. If one uses the silicon waveguide in its transparent region, then one cannot make use of the usual phonon-assisted interband transition as a detection mechanism.

One can alter the properties of an optical guided wave by changing either the real or the imaginary part of the refractive index *n* of either the guiding layer or the neighboring media. The former will be more effective because the electric field of the guided wave is concentrated within the actual guiding layer (see Figure 2). One hopes to cause such a change by applying an electric field induced by properly placed electrodes. Refractive effects—those associated with the real part of *n*—will likely be preferable to absorptive effects—those associated with the imaginary part of *n*—since the latter give rise to heat dissipation in the material.

Soref et al.[22] recently considered two types of refractive effects: electric field effects and charge carrier effects. The first, termed *electrorefraction*, is associated with electric-field-induced tunneling between the conduction and valence bands. The second is somewhat more complicated because of several mechanisms by which charge carriers can change the refractive index. Three such mechanisms are simple free-carrier effects, carrier interaction with impurity centers, and bandfilling. The analysis shows that carrier effects lead to larger changes in the refractive index of silicon than does electrorefraction. For typical parameters, for example, if carrier injection is used to change the carrier concentration by 10^{18} centimeters^{-3}, the refractive index of silicon is predicted to change by about one part in one thousand for an assumed optical wavelength of 1.3 micrometers. This is a sufficiently large effect, in principle, to be useful for devices. In fact, Kaneda et al. recently reported the performance of a free-carrier silicon waveguide modulator used at the optical wavelength 10.6 micrometers.[23] Further work is required to evaluate the full potential silicon offers for optical modulation.

Optical emission from crystalline silicon can be achieved using impurity luminescence. This has been demonstrated on many occasions, but only recently has anyone examined the efficiency of this process. Ennen et al. have reported that silicon implanted with erbium gives rise to room-temperature emission at the optical wavelength $\lambda = 1.54$ micrometers.[24] The emission spectrum from rare-earth elements, such as erbium, is rather insensitive to the properties of the host solid, and they obtained similar results for erbium implanted in other semiconductors as well. Although the authors were able to fabricate electroluminescent devices,[25] the low external quantum efficiency ($\sim 10^{-4}$) will limit the usefulness of these devices.

One type of impurity luminescence that shows promise involves the radiative decay of *excitons* bound to *isoelectronic* impurities in silicon. An isoelectronic (or isovalent) impurity complex is one in which the valence requirements of the silicon lattice are satisfied, leaving a neutral impurity site. Such a complex can bind an electron-hole pair (an exciton), which subsequently radiates. Isoelectronic bound exciton (IBE) emission typically exhibits a high internal quantum efficiency, since the neutral character of the complex leaves the exciton rather stable against nonradiative Auger recombination. Whereas the IBE emission mechanism was well known in gallium phosphide for many years, it was first identified in silicon as recently as 1979 in connection with an indium-related impurity center.[26] To date, only a handful of such impurities have been identified in silicon.

The external quantum efficiency of IBE emission from silicon is surprisingly high. Recent measurements have shown efficiencies as high as five percent in edge-emission geometries, a surprisingly large value for a semiconductor. Furthermore, this impurity luminescence can be excited electrically with relative ease. The one drawback at present is that most of the isoelectronic impurities reported in the literature support bound exciton emission only at low temperatures. There has been recent progress on this issue, however. A newly discovered, sulfur-related complex in silicon gives rise to optical emission near the wavelength $\lambda = 1.32$ micrometers.[27] The emission intensity reaches a maximum at $T \sim 80$ degrees Kelvin and is visible out to $T \sim 180$ degrees Kelvin. Figure 7 shows the emission spectrum from the sulfur-related complex at two temperatures. This positive result suggests the hope that we can indeed find an impurity complex that supports efficient optical emission at sub-bandgap wavelengths and is stable at room temperature.

Impurity luminescence is a convenient mechanism for fabricating devices. One can imagine implanting a small section of a silicon wafer with the proper impurity in order to define a source. If the silicon is itself an optical waveguide, as with the silicon-on-insulator geometry, the excited impurity will decay by emitting energy carried by the optical waveguide mode. This has already been demonstrated by implanting beryllium (Be) ions into an epitaxial silicon waveguide (see Figure 3c). Beryllium pairs form an isoelectronic complex in silicon that supports narrow-band, bound exciton emission at the wavelength $\lambda \sim 1.15$ micrometers for temperatures $T < 80$ degrees Kelvin. Once excited, either electrically or optically, the Be impurities did in turn excite the optical waveguide modes, as expected. This was clearly evident as a distinct edge emission from the epitaxial waveguide layer.[28]

This demonstrates that one can not only generate light within silicon, but can also transport the emitted energy across the silicon wafer in the form of optical waveguide modes. Taken to its most optimistic conclusion, this could have important consequences for future interconnection technology.

Silicon can be modified in several ways to allow the absorption, and hence detection, of photons with energy less than that of the indirect energy gap. Temkin et al. have recently demonstrated high photoconductive gain at $\lambda = 1.3$ micrometers in Si-Ge$_x$Si$_{1-x}$ strained-layer superlattice detectors formed on silicon substrates.[29] The strain inherent in these structures reduces the bandgap to permit the absorption of near-infrared radiation.

Platinum silicide (PtSi) Shottky-barrier detectors offer another approach to sub-bandgap detection. Quantum efficiencies greater than 10 percent have been reported for the wavelength range 1 micrometer $< \lambda < 2$ micrometers for such detectors,[30] and greater efficiencies might be obtained with an optical waveguide, though no one has yet reported such experiments. So, while there is reason for some optimism about sub-bandgap optical detection in or on silicon, there remains a great deal of work to do to establish the level of performance each technology can provide.

It is much too early to make specific predictions about how silicon-based integrated optics and optoelectronics might make an impact on the electronic computing arena. We can say, however, that the possibility of delivering information to, transporting information across, or extracting information from a silicon chip or wafer on an optical carrier seems attractive. Whether the optical signal originates from impurities within the silicon itself, from a III-V device formed on top of the silicon, or from some external source remains a detail for continued exploration.

The central idea behind the wavelength demultiplexer concept that appears in Figure 4 could, in principle, be implemented in a SIMOX waveguide instead of glass and redesigned to function at sub-bandgap wavelengths. This would introduce the possibility of having several, noninteracting, optical channels coexisting within the same piece of silicon.

It has already been demonstrated that high-performance electronic components can be fabricated in SIMOX wafers.[31] It is interesting to consider the potential advantages of optical communication between blocks of such components formed on a common SIMOX wafer. Such a configuration might be most attractive for wafer-scale integration, for which interconnection is a major issue. It remains to be seen whether this can be done in a practical way, but the possibilities are exciting. ☐

Acknowledgments

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IFIP Working Group 10.5 VLSI

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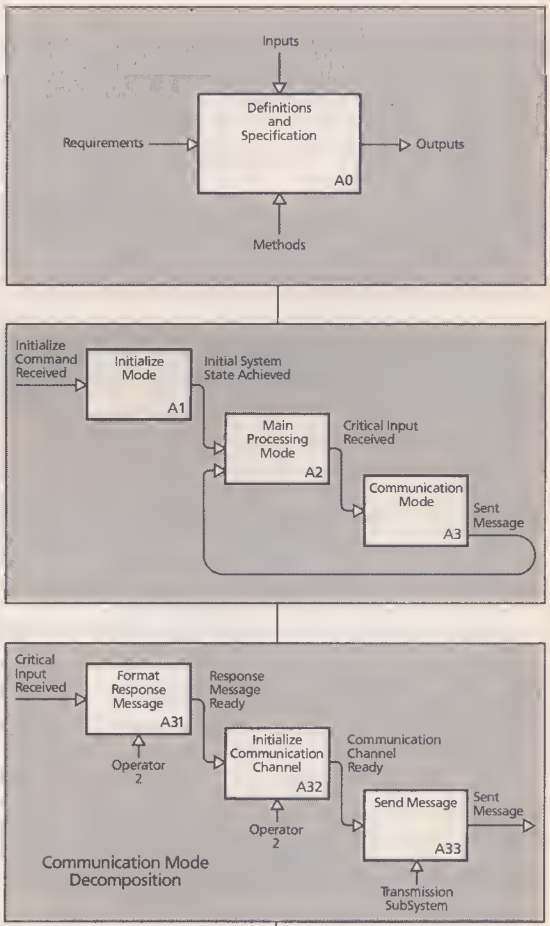

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Picosecond Integrated Optical Logic

Lawrence C. West
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An all-optical computer with 5- to 10-picosecond gate delays and one-gigabit memories won't be available tomorrow. But a direct path to its creation is known today.

Optical computing, like other areas of optics, was advanced by the invention of the laser in 1960. Throughout the 1960s many teams of researchers tried to make an optical gate with the newly discovered semiconductor diode lasers.[1,2] They succeeded in making some logic functions in the lower picosecond time scale, an impressive accomplishment for that time. But, because of inadequate materials and fabrication techniques, these speeds could only be sustained for microseconds before the diodes destructed from the tremendous power required.

This led, by the end of the 1960s, to R.W. Keyes' famous proposal[3] that optical logic was limited in speed by the large powers needed and dissipated in the material and, furthermore, that small computers could not dissipate this power. Keyes' paper sounded the death toll for optical computers for many years. It was still universally cited as the conclusive argument against optical computers when I began my research in 1977. During this period, however, research continued with bulk lenses and passive devices that did not require light to control itself directly. This form of computing has limited applications but, where applicable, as in a low-precision optical Fourier transform or a convolution, has great power simply because it is a good analog simulation of the desired function.

In the late 1970s and early 1980s, a resurgence of active optical devices occurred. Laser scientists focused on bistable devices in creating an active logic gate.[4] (See Figure 1.) Today, the concept of all-optical computing usually implies[5] two-dimensional arrays of optical bistable logic elements interconnected by a lens imaging between them. (See Figure 2.)

The approach discussed here uses all-optical nonbistable devices with integrated optical wiring instead of bulk optics. I know of no other proposal or experiment taking this approach, but it should provide most of the architectural flexibility of current electronic IC-based computers and be much faster. This article discusses first the advantages of its wiring over that of a lens-based system, then shows a method for achieving this integrated optical wiring. Next, it examines the properties of nonlinear optical materials and shows that a particular effect, the quantum well envelope state transition (QWEST), has the required properties. Finally, it outlines a method for creating an all-optical computer with 5- to 10-picosecond logic gates and gigabit memories.

Lenses vs. optical wiring

Why optics? It is important to review the rationale for using optical logic gates, especially considering the problems associated with any fundamentally new technology. Although proponents of the lens approach claim the major advantage is architectural, at the device level the major advantage is speed. Electronic transistors have operated down to the picosecond range, but optical pulses have been switched down to the 10-femtosecond range and can be easily handled with these bandwidths. Furthermore, all problems caused by inductances, resistances, and capacitances disappear. Connectors can handle multi-terahertz bandwidths with ease, and gate fan-out has no effect on device speed.

Usually, limitations on device speed reduce to the underlying physical effects of the interacting material. The reaction time of optical materials can vary widely, from

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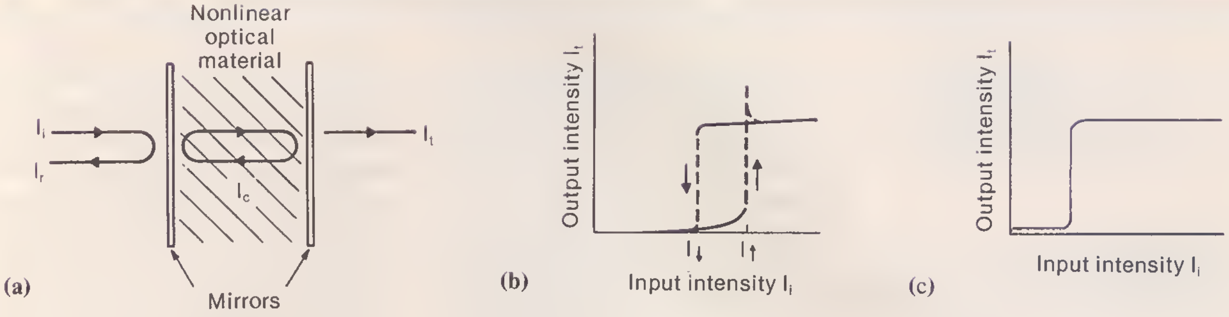

Figure 1. Illustration of a Fabry-Perot cavity with a nonlinear optical material (a). If the absorption per pass of the nonlinear material is greater than eight times the transmission *T* of the mirrors, then the Fabry-Perot will exhibit hysteresis in its output vs. input (b). The two solutions correspond to two states. In one the material is highly absorbing and not letting light into the cavity; in the other the light has entered the cavity and bleached out the absorption of the nonlinear material, allowing a high resonance cavity with high fields. The hysteresis is not necessary for logic, however. By making cavities with lower loss and other changes, the output could and should be made to look more like the ideal logic function (c).

hours to femtoseconds. But the higher speed picosecond and femtosecond range is the area of advantage for optical logic. Electronic logic currently handles the slower speeds very well and at a cost so low that optical logic technologies would have difficulty competing.

From logic gate to computer. Naturally, one would want and expect a faster logic gate to give a faster completion time on a given programming task. However, that is not necessarily the case. Two additional obstacles lie between logic gate speed and program speed. The first, at the hardware level, is the simple propagation delay of the signals. Second, for a given task, matching the architecture to the problem can be more significant than the base technology.

Propagation delay. For maximum computational speed, the propagation delay from one gate to the next should be much less than the logic switch time. In addition, the propagation time of the signal across the computer should be small compared to the maximum time spent in local calculations. With today's computer architectures, 10 to 40 logic operations can be performed locally during each global communication without sacrificing computer speed. But lens-based systems become severely propagation limited, with proposed systems[5] having propagation delays as much as 1000 times larger than the logic gate speed. (See Figure 2.)

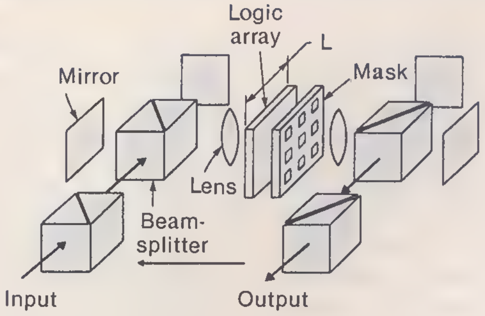

Figure 2. The common concept of an optical computer today consists of several logic arrays interconnected by lenses and beamsplitters imaging between them.

The system throughput, however, can remain high if each process remains sufficiently synchronous so that multiple processes can run behind one another without any process interfering with another. This synchronicity can indeed occur for lens-based systems, with each process actually a wafer of light moving through the system, as long as time-mixing optics (such as holograms) are not used for interconnects and random feedback is not a factor. Lens-based systems thus appear to provide a mechanism for using the computational power of high-speed gates without requiring small computers. But note that each process does indeed work slower, with each process transiting a logic gate only once each time it coincides with a logic array as it travels through the system. The system merely executes more independent processes piped into the optical path. If a given process cannot perform faster, no computational performance is gained from fast gates.

Using multiple microprocessors, a computer could be built today that would have the same computational performance as most of the lens-based picosecond optical logic systems proposed—and at a fraction of the price. Because lens-based systems are transit-time limited to times comparable to electronic logic, their performance is no better, no matter how fast the logic gate may be.

Architectural match. The second step in creating an optical computer from a logic gate is one of architecture. The biggest—and often-cited—advantage for lens-based architectures is massive parallelism. Proponents[5] envision millions of light beams connecting a large array of optical logic gates in parallel without interference. The claim is that this parallelism, simply because of the many interconnections allowed, will break the von Neumann bottleneck and thus lead to more powerful computers. The belief that the level of interconnect possible with optical lenses cannot be found in electronic wiring approaches propels investigation of the optical approach as a major technical advancement in computer architectures. But lenses also have the property of imaging light in a very regular fashion. So, although a lens provides a massive interconnect, it leaves little choice as to the location of these highly regular connections.

If this symmetry could not be broken, a lens-based computer could not be created. The current method for allowing arbitrary logical connections uses the optical logic gates themselves in combination with optical beam splitting and translations to choose the connection. Unfortunately, this is not an efficient process, and the number of logic gate passes needed for communication is approximately three to 10 per useful logic operation on the signals.

Communication density. Another advantage claimed for optics is the ability of one beam to pass through another in free space, thus allowing more communication channels per volume. But the volume needed to image between two arrays is equivalent to that of a wire having the cross section of the logic gate and the length between the arrays for each logic gate. That length, however, is several times the dimension of the system, and several propagations between arrays may be needed for irregular communication. In contrast, a wire-based computer needs only a wire of the length between the gates that need to communicate, usually 10 to 100 times smaller than overall system dimensions. Using a lens actually increases communication volume 10 to 100 times over that of a wire-based system. So the parallelism provided by the lens is not free and has a trade-off with the propagation delays, already severe enough. The same parallelism can be obtained with an optical wire-based computer with much less volume and fewer propagation delays.

Normally, a computer distributes the logic gates over many two-dimensional surfaces or boards. The expanded surface area allows for greater heat dissipation. This is especially important for optical logic devices, since their high speeds require very high powers. But the logic of lens-based systems is confined in highly compact two-dimensional arrays. Unless logic switching energies can be improved a thousandfold over current levels, the inability to dissipate heat will limit gate times to one-nanosecond or slower.

Lens-based uses. The foregoing does not mean that lens-based systems cannot perform useful computing tasks. For the computing in switching systems, for example, a lens-based computer is perfect. It switches lines quickly, and its long latency in propagation delays becomes unimportant, since the propagation delay in the communication to the computer is already very large. The lens-based system's ability to handle the very high bandwidths unobtainable in electronics is essential to future communications systems.

In addition, as computers become massively parallel, intercommunication systems may look more like switching computers, for which lens-based systems perform nicely and with extremely high bandwidths.

I do not question the utility of lens-based systems, I merely question their use for high-speed general-purpose computing tasks, especially those not easily made parallel.

Integrated optics

The question now is how to put the advantages of integrated optical wiring to use. Typically, an optical wire or waveguide is created by confining the light to a material with a higher index of refraction than its surroundings. The light then stays confined by reflection off the walls at an angle steeper than can be refracted out of the waveguide, so no light escapes. Using this mechanism, optical fibers transmit signals hundreds of kilometers without significant loss.

Current approaches. The problem is that current integrated-optics technology is nowhere near as compact as needed to integrate 10^6 optical logic gates in a volume as small as a cubic centimeter. For instance, a current distributed-feedback mirror on a typical diode laser can be hundreds of micrometers long, making the entire laser most of a millimeter. At best, a 90-degree bend takes hundreds of micrometers of length. None of these dimensions even remotely approaches sufficient compactness for the high densities required. Therefore, something dramatically different is required.

Both of the above components are large for the same reason. The refractive index of the outside cladding material is close to that of the waveguide. The index change is often as small as 3.50 to 3.55, or about one percent. Because of the small index difference, the radius of a waveguide curve cannot be too small, or the light in the waveguide cannot be totally internally reflected at the interface. Similarly, the mirror must be long enough that a sufficient number of surfaces, each with a small perturbation because of the lower index difference, can add up to a significant reflection.

Compact optical devices. It would seem that the solution is to clad the waveguide with a much lower index material, so as to increase the difference between the waveguide and the cladding. This is not done for several reasons. First, for a single-mode waveguide, the waveguide dimension would need to be smaller than the wavelength in the material (0.25 micrometers in gallium arsenide (GaAs)), and this dimension is currently very difficult to fabricate lithographically. Also, for reflectors, the long dimensions are sometimes desired because they give a narrow bandwidth—the opposite of optical computing needs. But, most importantly, the surface scattering increases tremendously as the refractive index between the cladding and waveguide increases, and scattering is already a major loss factor for dielectric waveguides.

Although the surface scattering increases dramatically with the index difference, it also decreases rapidly with the ratio of the surface perturbation distance to the wavelength. To compensate for the increased surface scatter from larger index differences, the surface smoothness on all sides of the waveguide would need to be improved tenfold or more (to a smoothness of 0.01 to 0.03 micrometers for near-visible light). This is generally beyond current fabrication ability, especially for production chips. But increasing the wavelength tenfold has a similar effect; combined with a small improvement in waveguide smoothness, it would eliminate waveguide scattering altogether.

At first, it might seem that all the one-micrometer wiring has now turned into 10-micrometer wiring with 10-micrometer infrared radiation in the waveguides. But that is not the case. Rather, the resulting structures are exactly what one would hope to manufacture, namely lines of about two- to three-micrometer width, which are easy to pattern and still give relatively high densities of needed components.

What happened? First, the 10-micrometer light became three micrometers in the materials of interest, because of the large index of refraction in these materials. Furthermore, with high index differences, the waveguide dimensions can and must be smaller to obtain single-mode waveguides. With very large index differences, waveguides with dimensions of a half wave are not unreasonable. As one reduces the wavelength to below one micrometer, the waveguides can be made as small as 0.1 to 0.2 micrometer, assuming sufficient lithography exists. Also, these small waveguides have multiterahertz bandwidths, even for long wire lengths. The same cannot be said for electronic wiring, where a one-micrometer wire is limited to gigahertz bandwidths across the dimension of a wafer, and a 0.1-micrometer wire would be restricted to the megahertz range for similar distances.

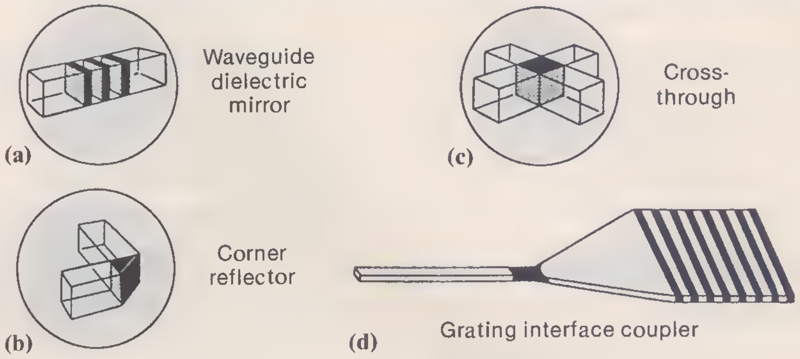

Figure 3. Various components being developed for integrated optical computers: (a) a waveguide 90-percent reflecting mirror constructed of alternating quarter-wave layers of zinc selenide and germanium etched across the full waveguide; (b) a waveguide corner turning the infrared light at a right angle by total internal reflection within the germanium prism; (c) a cross-through with a higher index medium containing the light in the waveguides across the boundary, allowing signals to cross in one plane: (d) the coupler between the small waveguides and the external beams, consisting of a taper up to a large dimension (75 to 100 micrometers) grating, which couples light out normal to the surface in a Gaussian profile beam for coupling to lenses or to other boards directly above or below.

Example components. As some example components show, the use of large-index-difference waveguides changes much of how integrated optics is approached.

Mirror. First, consider an integrated optical mirror. Instead of perturbing the surface, etch a deep pit entirely through the waveguide and fill it with a very much larger refractive material (see Figure 3a). With large refractive index materials such as zinc selenide ($n = 2.4$) and germanium ($n = 4.0$), this reflection can be rather large. With a stack of three quarter-wave pits or six surfaces, one can achieve much better than a 90-percent power reflector. The three pits will have an overall length of about five micrometers.

Waveguide bends. Take as a second example a 90-degree bend. If we use a high-index material such as germanium ($n = 4.0$), then light is totally internally reflected with an angle more than 15 degrees away from normal incidence. Thus, if we put a prism of germanium at the corner (see Figure 3b), the light incident at 45 degrees will be mostly reflected around the corner.

Crossover. Also of importance is the ability of light to cross other beams without interference in the same signal plane (see Figure 3c). This crossover ability should greatly lower the number of signal levels required, to as low as one for small- and medium-scale integration. As densities and wiring increase, multiple wiring planes can be grown on top of one another with coupling between them accomplished by typical coupling techniques such as delta-beta couplers oriented vertically instead of horizontally between guides.

Coupler. A crucial integrated optical coupler, on and off the chip, is one of the hardest components to develop. Starting from a 2.5-micrometer integrated optical waveguide, the beam is expanded within the plane of the integrated optics with an integrated optical lens (see Figure 3d). The wide and flat infrared beam must now be coupled out of the wafer into a circular beam projecting normally from the surface. This task is especially appropriate for a grating coupler, which, like a diffraction grating, scatters light coherently from the waveguide into free space, preferably normal to the surface.

By proper tapering of the coupling strength out of the waveguide, a Gaussian profile light beam with a diameter of 50 micrometers can be created. The large diameter allows for obstruction with dust particles up to 20 micrometers in diameter and for tens of micrometers position error and expansion allowance. Greater tolerance could be achieved with a larger diameter coupler, but only at the expense of chip area, which is already dominated by couplers for small wires and logic gates. The infrared beam could propagate for a distance of about 200 micrometers in free space from the surface of the wafer before diffraction expands the beam and it needs refocusing. This gives plenty of gap tolerance, enough to allow contemplation of direct interboard connection without going through a backplane or edge connector.

Note that the connector considered is a surface connector, not an edge connector. As such, it allows for very high connector densities, limited only by the real-estate cost of the connector itself.

Optical nonlinear materials

Creating an all-optical logic function requires finding a material that allows light beams to affect one another at low power. The power of a logic gate should be so low as to be limited only by signal levels with sufficient quanta for reliable operation. As the number of quanta representing a signal in a system is lowered, the relative shot noise level increases. It can be shown that one must have approximately 300 quanta to prevent a false signal from quantum noise. Because a logic gate must have fanout, the power supplied to the logic gate will be on the order of 10 times larger than the power in each of its signal inputs. Thus, the minimum power gate currently contemplated is powered with about 3000 quanta per switch.

This argument is equally valid for electronic or optical logic. The minimum energy needed is the minimum quanta times its energy. For electronics, an electron dropping through a voltage of one volt uses an energy of one electronvolt. For photons, the quanta of light, the energy is inversely related to wavelength. The constant of proportionality is the product of Planck's constant, h, and the speed of light, c. This product, hc, is equal to 1.24 electronvolt-micrometers. Visible light at 0.5 micrometers has a quantum energy of 2.5 electronvolts. The wavelength proposed here for integrated optics is 10 micrometers, which has a low quantum energy of 0.124 electronvolts.

Note that, in practice, the optical and electrical quantum energies are similar—in the 0.1 to 5 electronvolt range, with the higher values being more common today. If a logic gate were to consume 3000 of these quanta per switch, its energy per switch is easy to calculate, remembering that an electronvolt equals 1.6×10^{-4} femtojoules. A logic gate working with one-electronvolt quanta will run into quantum statistical problems at around 0.5 femtojoules. A logic gate working with 0.1-electronvolt quanta (proposed here) will be able to go 10 times lower in energy to 0.05 femtojoules before running into quantum statistical problems.

It is important to note that the older superconducting logic had voltages in the millivolt range and had plenty of quanta. Logic with the newer superconductors, if it approaches room temperature, will approach transistor-device voltages and will, therefore, have the same limitations. For a picosecond gate, the minimum power is 0.5 milliwatt with one-electronvolt quanta and 0.05 milliwatt with 0.1-electronvolt quanta. Creation of picosecond logic much below these power levels will require improvement of quantum mechanical statistics of signals.

Optical nonlinear processes today have switching energies on a par with experimental electronic logic devices, that is, tens of femtojoules per square micrometer. This energy can be improved another factor of 100 to 1000 before running into the signal-level problem described above, and much of how to get there is known.

Properties. Two light beams can interact in a material in several ways. A simple way is for one light beam to illuminate a photodetector to create a current, use electronic transistors and logic, then modulate another beam with the electrical output. This method was not taken because the speed of the logic will remain limited by the electronic transistor. Although some intercommunication gains result, a better method is creating an entirely optical gate with a capacity for operating orders of magnitude faster than electronic gates and using the optical wiring to carry the high bandwidth signals. One then needs a material that allows light to affect its properties, usually refractive index or absorption, which in turn affect another light beam.

These optical properties of a material arise from optically induced electron transitions between the quantum states of the material. Changing these properties usually requires moving significant numbers of electrons between states to change resonances. Both the coupling of the resonances to the optical beam and the effect of the optical beam on the transitions between states are described by one simple quantity, the oscillator strength f, which is the ratio of the response of the material to that expected from a free electron or one bound as a harmonic oscillator. The oscillator strengths of atomic and molecular transitions are usually below unity. But the semiconductor materials have oscillator strengths in the 10 to 100 range. In direct bandgap systems, the oscillator strength of a semiconductor is usually found simply by the ratio of a free electron mass to the effective mass of the semiconductor conduction band.

Resonance transition. Interaction with the light frequency that is significantly off-resonance from the transition frequency of the interacting states has the advantage of not requiring the material to absorb much of the light. Furthermore, the speed of an off-resonance transition can be as fast as the off-resonance frequency, or hundreds of terahertz. This off-resonance interaction is used commonly today to view 10-femtosecond optical pulses.

This speed, however, comes at a steep price in power required. It can be shown that the power increases as the cube of the off-resonance frequency. In practice, these off-resonance frequencies must be very large because of other material absorptions in the range of interest, as well as the width of the absorption lines themselves. The powers can be lowered only with long propagation distances and times—undesirable in a fast computer. As the light becomes resonant, the response of the material becomes slower, limited by the lifetime of the upper state $T1$ rather than the off-resonance frequency. Also, since a competitive optical logic device needs to work in the femtosecond and picosecond range and the radiative transition times in the visible and infrared are tens of nanoseconds or higher, the absorbed power must be dissipated nonradiatively, which generates heat inside the computer.

In spite of this problem, this near-resonance interaction is the preferred method of operation for an optical computer. First, because $T1$ times can be very small, to the hundreds of femtoseconds or better, the speeds desired can be achieved with this approach. Also, the power to be dissipated can be made fairly small and can be reasonably handled. And most importantly, it greatly lowers the power requirements of the optical power supply, the most expensive component of any optical computer. As the light becomes exactly on resonance, the index of refraction goes to zero, and the absorption of light is the mechanism for interaction.

Index/absorption change. For on- and near-resonance interactions, a simple formula gives the energy needed to create sufficient population in the upper quantum state for a given change in index or absorption. A material optical energy, E_0, is defined by

$$E_0 = \frac{\lambda\hbar\Delta\omega(m)}{n f}\,\frac{mc^2 2\pi\epsilon_0}{e^2}$$

where λ is the wavelength of the light, $\hbar\Delta\omega(m)$ is the material linewidth, n is the refractive index, f is the oscillator strength, m is the free electron mass, c is the speed of light, ϵ_0 is the free-space dielectric constant, and e is the electron charge. The first group of parameters contains all the material-dependent quantities. As an example, let λ = 1 micrometer, f = 10, n = 3.6, and $\hbar\Delta\omega(m)$ = 1.0 milli-electronvolt, typical numbers for a GaAs exciton. Inserting into the above equation yields E_0 = 0.79 femtojoules.

Logic gate energy depends on the amount of phase shift or absorption change needed to create an on or off signal. If a logic gate works with a phase shift of $\Delta\phi$ or a net induced absorption of Δa, then the power needed to induce these effects with the laser wavelength tuned to the peak index of refraction or else the peak absorption is $4E_0\Delta\phi$ or $E_0\Delta a$, respectively. This definition assumes that the light was focused to a diameter of λ/n. If we use an ideal Fabry-Perot cavity with mirror transmissions of T, the phase shift needed in the cavity to create a transmission change of a factor of five is given simply by $\Delta\phi = T$. So an exciton in GaAs working in a cavity with 90-percent reflecting mirrors will need only 0.079 femtojoules to switch.

In practice, the energies are much higher, at the picojoule level.[7] The primary reason is spot size. For the GaAs exciton, the minimum spot size of λ/n is about 0.25 micrometers. Experimental spot sizes are many micrometers, raising the energy a couple of orders of magnitude. Also, impurity absorptions and other effects prevent the use of light at the peak refractive index; usually the light is tens of milli-electronvolts away from the resonance, instead of one milli-electronvolt. Also, only the best materials have exciton linewidths of only one milli-electronvolt; often they are three milli-electronvolts or higher. Furthermore, the small Fabry-Perot cavities made need large changes in refractive index to switch. With these large changes in index, the exciton saturates, and the index change must come from the more distant and more energy-broadened free electron energy resonances. Finally, the bandgap renormalizes and tends to cancel some of these effects as the semiconductor fills with electrons. Minimum spot sizes and higher reflectivity cavities will eliminate some of these effects and dramatically lower the power.

The QWEST nonlinear material has a demonstrated linewidth of three milli-electronvolts, oscillator strength of 12, refractive index of 3.3, and wavelength of 10 micrometers.

The QWEST (quantum-well envelope state transition) nonlinear material, described later, has a demonstrated linewidth of three milli-electronvolts, oscillator strength of 12, refractive index of 3.3, and wavelength of 10 micrometers. Thus, its minimum switching energy for a Fabry-Perot cavity with 10-percent transmission mirrors is about 2.15 femtojoules. With gain and losses included, the energy requirements of the logic gate would be about 10 times higher, or 21 femtojoules. But, unlike devices that interact with the bandgap, QWEST is sufficiently ideal to possibly achieve these minimum energies.

Dielectric resonance. If the minimum power cannot be obtained directly from the nonlinear material, many enhancements can be made to bring the signal powers to the quantum noise limit. One such enhancement is the Fabry-Perot interferometer with mirror transmissions of T. For a given external power, the power inside the Fabry-Perot cavity is $1/T$ times larger than the incident power. More importantly, the phase shifts and absorptions needed to switch are reduced by a factor of $1/T$, as illustrated above. The Fabry-Perot also has the effect of improving contrast of on to off signals, which is important for logic gates.

The Fabry-Perot is not the only resonance that can be used. Surface plasmons, which exist at the interface between a metal and a dielectric, can also enhance the power internally. Small (tens of nanometers) round particles with dielectric constants of −2, which exist in metals, have been observed to enhance the nonlinear optical scattering from molecules on the surface by as much as a millionfold.[8] If the nonlinear material can be sandwiched between another material with the opposite dielectric constant and thicknesses less than the wavelength, then the net refractive index of the material is zero or infinity, depending on the polarization, and an enormous reduction in gate power should result. These negative dielectric constants are seen in all metals and semimetals for wavelengths from the visible to the far infrared. The speed of these dielectric resonances is limited only by the transit time of light across their submicrometer dimensions, which is femtoseconds.

These resonances are well understood and observed in practice. The only problem is using them to construct a realizable logic gate with low loss and good logic function. These enhancements, in total, lower the power requirements of a logic gate over eight orders of magnitude. But with the quantum limited energies of the nonlinear materials, E_0, only two or three orders of magnitude away, it appears almost certain that some enhancement or combination will soon reach the quantum statistical limit in a practical device.

Semiconductor problems. Semiconductors are popular nonlinear optical materials because of their large oscillator strengths and their high degree of thermal conductivity, important for removing heat. One of the problems with semiconductors is that the normal valence-to-conduction band transitions do not relax very fast. The GaAs excitons radiatively relax in 10 nanoseconds. With the use of interface recombination, relaxation in GaAs has been reduced to 20 picoseconds. But these numbers are still far from the hundreds of femtoseconds desired for fast switching. Also, the semiconductor bandgaps have a strong temperature dependence. In GaAs, the bandgap changes 0.5 milli-electronvolts per degree Celsius. If a GaAs exciton resonance were used at peak refractive index, a Fabry-Perot cavity would shift with only a degree or two temperature change.

Note that these logic gates will absorb milliwatts of random power in a region of only 0.25-micrometer diameter, creating temperature fluctuations of tens of degrees Celsius. This effect occurs in practice, and logic gates are usually tested with very low duty cycle lasers (one thousand to one) to prevent thermal switching. These problems have led some researchers to concentrate on slower gates with hundreds of picosecond speeds, which are only marginally competitive with electronic logic. Also, bandgap operation in semiconductors has the problem of impurity absorption, which will be very difficult to eliminate.

In view of these problems, a theoretical search was conducted in the late 1970s and early 1980s of many types of materials. Semiconductors have the overwhelming advantage of high thermal conductivity and oscillator strength, but the long lifetime and temperature sensitivity problems cannot be eliminated in bandgap transitions. Also, a mid-infrared transition would allow compact integrated-optical waveguides, as discussed earlier, and permit use of the inexpensive CO_2 lasers to power the computer.

One solution is to use transitions entirely within the conduction band. They show orders of magnitude lower temperature dependence and relax quickly (100 to 400 femtoseconds) by simple electron-electron scattering. But the quantum energies of the free electrons within the band are very broad. Impurity transitions have too low an oscillator strength, relaxation rates, and quantum energies. Nonlinearities from free electrons in nonparabolic bands are very low. But electrons in quantum wells have an interesting property. Normally the transitions between electrons in different bands are broad because the energy of the electron increases with momentum given opposite signs in the two bands. But within the band, the electron energy as a function of momentum increases equally for two different quantum well states, since they have the same effective mass. If momentum is conserved, transitions for free electrons with all energies have only one transition energy, or the linewidth is narrow and lifetime broadened. Furthermore, the transition energy is in an otherwise highly transparent region of GaAs, providing an isolated resonance to work with. The resonance also can be created anywhere from two-micrometer wavelengths to the microwave and beyond.

In GaAs, the transition is between the lowest quantum well states.[9,10] The envelope of the wavefunction of the states is illustrated in Figure 4. The full wavefunction includes a multiplicative part that is periodic with the lattice spacing (not shown). If the light is polarized normal to the quantum well planes, then a fully allowed and very large (two nanometers) dipole exists between the envelopes of wavefunctions. For this reason, this particular type of inter-subband transition is called a quantum well envelope state transition.

Optical computing is presumed to be a major application of bistability. Unfortunately, bistable operation is one of the worst ways to create a logic gate.

QWEST. The quantum well envelope state transition (QWEST) has a measured and theoretical oscillator strength of 12 on the transition between the lowest states (one to two). The next transition (two to three) has an oscillator strength of 20. The transition has now been observed by several researchers[9-11] with linewidths in the 3 to 10 milli-electronvolt range. The linewidth is believed to be lifetime broadened as it has a Lorentzian spectrum. Several femtosecond studies of quantum wells indicate this, and a direct measurement of the QWEST lifetime is being conducted using the beat frequency between two broadband (six terahertz) tunable CO_2 lasers.

As predicted, QWEST operates over a 0- to 400-kelvin temperature range, with little change seen in its resonant energy and bandwidth. (See Figure 5.) The change in QWEST energy with temperature is about 0.015 milli-electronvolt per degree Celsius, or 30 times less sensitive than bandgap transitions, and it can be adjusted to near zero if needed. QWEST has now been used to create an infrared photodetector[11] and a modulator, and for second harmonic generation. The modulator and detector are capable of directly interfacing the 10-micrometer infrared light signals with the normal electronic logic levels.

In addition to the nice physical properties, QWEST exists in GaAs quantum wells, a technology currently being developed for high-speed electronic transistors.

Logic gates

Attempts to incorporate nonlinearity into a logic gate have met with little success, primarily because of confusion as to how logic should be performed. Take, for example, the scientific community's attempt to create and enhance optical bistability in Fabry-Perot cavities for use as logic (Figure 1), and recall the numerous conferences held and books written on this subject.[4]

Optical computing is presumed to be a major application of bistability. Unfortunately, bistable operation is one of the worst ways to create a logic gate. Not only does the threshold nature of these devices make mass production difficult, but their gain, contrast, fan-in and fan-out are generally very poor. The latching nature of the bistable device, from which the name "bistable" originated, is a detriment to any high-speed logic device; to reset, it must wait for some power beam to drop back. But, more importantly, optical logic can be made without bistability.

Bistable alternatives. As an alternate to bistable logic, it is possible to build optical logic in which the output is controlled by the input in a deterministic fashion, with good isolation and saturation levels. One example is the laser saturation logic created in the 1960s.[1,2]

The function needed from a logic gate is gain and saturation. Bistability was born with the lack of any inputs on a gate other than a power supply, which was modulated. But once a second input is allowed (and this input is not only allowed to be different but should be), several possibilities are seen for deterministic control, even in a Fabry-Perot cavity.

A Fabry-Perot cavity offers advantages for optical logic in its ability to sharpen the effect of a linear change in refractive index and in its lowering of power requirements. The Fabry-Perot cavity is a very useful device, but it need not be used in the bistable mode. In fact, it performs better in the non-bistable mode. The transmission, or the ratio of transmitted to incident intensities, I_t/I_i, of a Fabry-Perot cavity with mirror reflectivities of R and transmission $T = (1-R)$ and absorption per pass of a and phase shift per pass of δ is given by

$$\frac{I_t}{I_i} = \left[1 - \frac{a}{1-R}\right] \frac{1}{1 + 4R/(1-R)^2 \sin^2\delta}$$

for a cavity on resonance $\delta = n\pi + \phi$, where ϕ is the extra phase shift per pass. If

ϕ is small, then the sinδ reduces to ϕ, and the above equation reduces to

$$\frac{I_t}{I_i}=\frac{T^2}{(a+T)^2+4R\phi^2}$$

It can now be seen that, to achieve a switch in a cavity with no absorption, the phase ϕ can be switched from 0 to T or higher. In a cavity on resonance with ϕ = 0, the absorption per pass can be switched from 0 to T or higher for a four to one contrast. Unfortunately, a and ϕ are neither pure nor independent. The absorption a is always nonzero because of residual absorption in the cavity and mirror imperfections. Also, if the nonlinear optical material has a Lorentzian spectral profile, the peak phi as a function of wavelength has a residual absorption of $a = 2\phi$ associated with the same resonance.

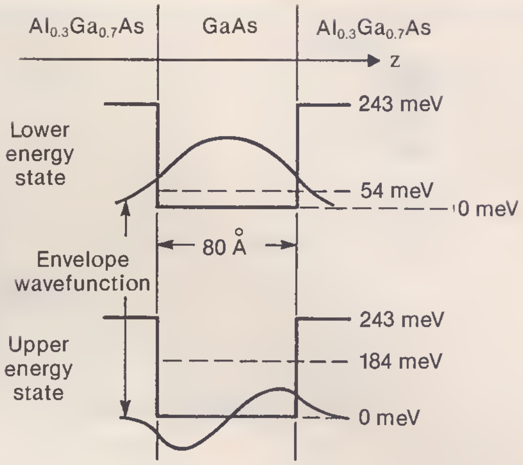

Figure 4. The quantum well envelope wavefunctions are illustrated along with the potential diagram of the GaAs conduction band with AlGaAs cladding. The electron energies become quantized and infrared transitions are made between them through the allowed dipoles of their envelope wavefunctions.

Only by going far from resonance does absorption become less significant. Residual absorption will cause the Fabry-Perot cavity to have about 50-percent peak transmission, even with the laser four linewidths away from the resonance. But the index is four times smaller this far away from resonance, increasing the power by a similar factor. In contrast, if the laser is tuned to the center of the absorption line, the induced phase will always remain at zero, and the gate will be switched entirely with absorption saturation.

Switching a gate with index changes thus raises the power of a logic gate sixteenfold over an absorption switch, fourfold because of the larger $4E_0$ given above, and another fourfold because the laser cannot be at the peak index for good cavity efficiency. But if absorption saturation is used to switch a cavity, the cavity will slowly saturate and become transmitting, giving poor logic function.

Logic function. A method for using the refractive index to create a logic gate is illustrated in Figure 6. This logic gate is a four-input NOR gate with compliment. This gate with no input is biased off-resonance by making a cavity slightly too short for resonance with an integer number of half wavelengths. When an input goes high, the cavity will see a change in refractive index that will bias it onto resonance. The power beam on the cavity will cooperate to bring the internal power in the cavity to proper bias for on-resonance operation; however, we are not in the fully bistable regime, which induces hysteresis. The gain in this cavity is not achieved by operation at a threshold as in a bistable gate, but rather by enhancing the coupling of the input into the cavity multifold over the power beam by creating a larger resonance for the input than for the power beam. Inside the cavity, the power and logical input will have nearly equal energies, even though the logical input power may be many times smaller than the power beam. The nonlinear material will then absorb nearly all of the input power, but only a fraction of the power beam. In the figure the input beam has more quarter-wave reflectors in its mirror than the main cavity to enhance its cavity reflectivity and coupling.

Optical interference. A problem for optics that does not exist for electronics is optical interference between inputs and the power beam. Since the light travels arbitrary distances between gates, the phase of the light is not known, yet it can interfere with the main cavity power either constructively or destructively with totally different effects. Mechanisms for eliminating this phase-dependent interference between beams involve time separation for pulsed logic, polarization separation, physical separation at different parts of the gate, use of orthogonal

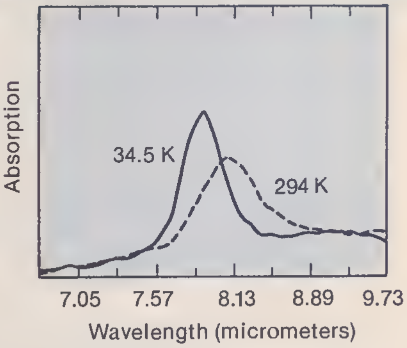

Figure 5. The absorption of GaAs is totally transparent in the infrared except for the new QWEST transition, which can be created anywhere in this range by adjustment of the well width upon growth. The temperature tolerance of the QWEST is illustrated by noting its small change over a 260-kelvin (470-degrees Fahrenheit) temperature range. The small changes seen probably would not affect the operation of a logic gate over the same range.

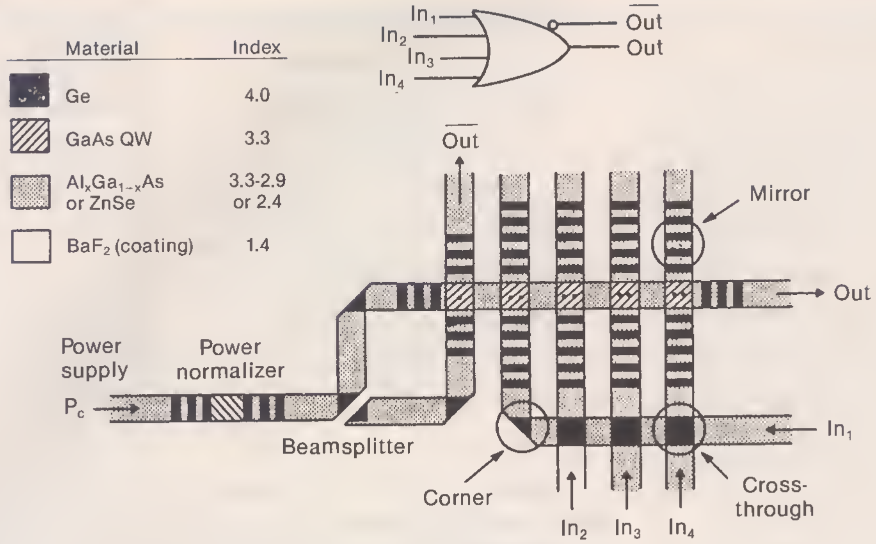

Figure 6. A prototype design of a logic gate using the various integrated optical components. Note that instead of achieving gain by thresholding the Fabry-Perot on the edge of a hysteresis jump, as is done with the bistable gates of Figure 1, this gate achieves gain by enhanced absorption in the Fabry-Perot cavity by using a cross cavity of even higher resonance on the input.

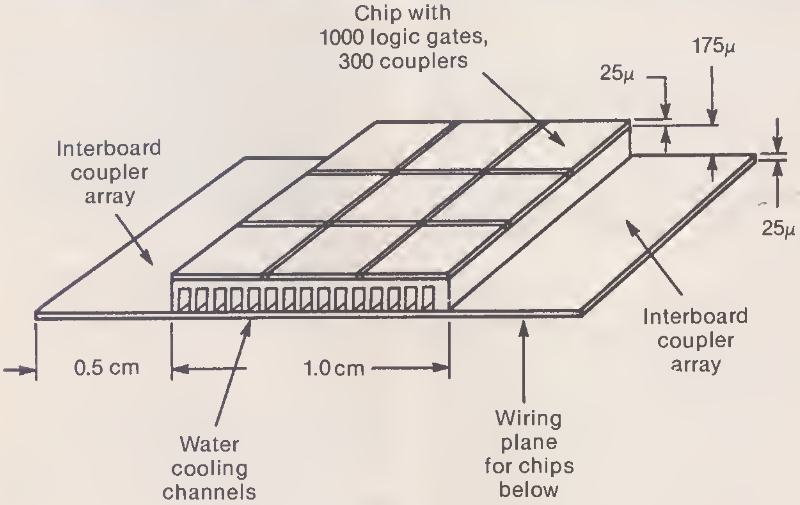

Figure 7. A logic board would be one centimeter square and contain on the order of 9 logic chips, measuring three millimeters on a side. The chips would be mounted on a cooling fin with channels for water cooling flow. The interconnection between the chips on the board is via grating couplers to a wiring plane fastened to bottom of the board above.

modes with gates insensitive to the particular mode pattern, and use of different wavelengths sufficiently separated to average the phases.

For our integrated optical logic using the QWEST transition, which must use continuous polarized light, we use the latter three of the above-mentioned effects. The waveguides only allow single transverse mode operation. The input interference with the main power beam in the cavity can thus be eliminated by overlapping the input mode over two adjacent antinodes of the main cavity. The adjacent antinodes have opposite phases, but the input has the same phase. Since the overall main cavity resonance is sensitive only to the sum of these two interferences, the relative phase of the input to the main power beam is now irrelevant to operation. The complement function is provided by yet another cavity intersecting the first, which is initially biased on resonance but is powered off when power exists in the main cavity.

This logic gate still has some problems, in the reflection of inputs back to the previous gate, for instance, and many further improvements are being made.

Computer systems

Although optical systems are far away, they must be considered in the decisions we make in developing the lower technologies. The infrared waveguide technologies we are developing have broad applications, pushing the technology base of current computers from the nanosecond to the picosecond range, with lower power and greater communication bandwidth. The first application will most likely be in special-purpose MSI (100 gate) chips directly interfaced with electronics and embedded within the electronic structures. The infiltration of the entirely optical computer will most likely start at the supercomputer level. Therefore, let's discuss how to build a supercomputer mainframe.

Building a supercomputer mainframe. The proposed logic gate is about 30 micrometers on a side, limited mostly by the two- to three-micrometer wires of which it is made. This gives it an area of about 1000 square micrometers. The grating coupler has dimensions of 150 micrometers by 75 micrometers, including the taper, for a 50-micrometer diameter light beam, giving it an area of 10^4 square micrometers.

Now, suppose we put 300 couplers and 1100 gates on a 3.3-millimeter square chip. The total chip area is 10^7 square micrometers. So the couplers consume 30 percent of the chip area, and the logic gates consume 10 percent, leaving 60 percent of the area open for wiring. The ability to cross wires in the same plane is expected to greatly simplify the wiring problem, and the wiring can be extended to multiple planes if needed. By placing nine of these chips on a board, approximately 10,000 gates can be put on a one-centimeter square board.

Interchip communication is performed with a wiring board, placed just above the logic. This wiring board contains no logic, only long-length wiring and grating couplers. It is placed on the bottom of the board just above the board to which it communicates (see Figure 7). It also serves as the bottom mechanical seal to the cooling channels, which are sandwiched between this wiring board and the logic board on top.

The thickness of the logic chip and wiring board is 25 micrometers. The cooling channels are 175-micrometers thick with a channel dimension of 50 micrometers by 150 micrometers. The overall board is 225 micrometers or 10 mils thick. Forty of these boards can be stacked on top of one another for a cubic centimeter computer.

The wiring boards will extend beyond the dimensions of the logic boards on two sides by an extra five millimeters to allow direct interchip communication between the wiring boards in free space. Also, the boards can directly talk to one another if the grating coupler is directly placed over a germanium cooling fin on the logic board. The 50-micrometer diameter signal beam can only talk to adjacent boards before diffraction expands the beam too large. The propagation distance increases as the square of the coupler dimension, with the largest interboard distance requiring a 350-micrometer diameter beam. Alternatively, the beam could be reimaged with a fresnel lens at some of the intermediate boards with some loss in efficiency.

The total number of interboard connections, with over 20,000 interboard connections possible on each of the 40 boards, provides more possible connectors than gates. Forty boards with 10,000 gates brings the overall number of logic gates to 400,000. Worst-case propagation distances are about three centimeters, some in free space. The speed of light in the zinc selenide waveguide is about half that of free space, or about 66 picoseconds per centimeter versus 33 picoseconds per centimeter in free space. The worst-case transit time is about 150 picoseconds across the computer. This propagation delay is considered compatible with anticipated five- to 10-picosecond gate delays.

Memory and interface. Memory interface is placed above the upper logic board. A fast one-megabit memory with 300-picosecond fetch time can be made with a free-space approach (see Figure 8). This memory on the upper board would consist of an array of 128 by 128 grating couplers, for a total of 16,000. Each of these couplers is paired with a neighbor for an input and output port. A lens and reflector then reimages the output coupler to the input coupler. The memory is then the light on the fly between the output coupler and the input coupler.

This fast memory will probably use faster gates than the logic (around one picosecond), and store 128 pulse widths in the path. The delay for access would then be about 250 picoseconds. Faster gates are used for this approach because of the increased memory available with the same structure, allowing for lower gate counts and more compact memories, especially important for transit times to and from the memory. This faster memory gate is possible because the nonlinear material is much faster than one picosecond.

Slowing logic gates to lower their power is usually a problem. (Slow gates are used for logic since the computer is believed to be mostly propagation limited, and thus some power can be saved.) On the board, between each input and output coupler, two gates refresh the leading and trailing edges of each light input relative to a master clock. In addition, two gates will be needed for the read and write decoding of the element. In addition to propagation time for arrival of the proper memory plane, there is a several-picosecond delay for decoding the memory address. The memory can be accessed one page at a time if needed, with 16,000 bits on a page. Finally, one of the major delays in this memory will, as before, be the 150-picosecond, worst-case, single-pass transit time across the computer.

This fast and relatively small one-megabit memory might be called a cache, supporting the numerous fast registers internal to the computer. In addition to this cache memory, the free-space memory concept can be carried out for even larger memories. For instance, increasing each dimension of the above array by a factor of about 10, to an array of 1024 by 1024 grating coupler pairs with a string of 1024 bits in time, would yield a gigabit memory with an overall access time of about 2.5 nanoseconds. Within this access time, one could access any number of memory elements, up to the maximum capacity of temporary registers or cache, by specifying a time-ordered list of the memory elements required. This larger memory would require over 10 times more optical power than the remainder of the computer, because of the faster gates needed for the 1024 by 1024 array of gates driving the couplers. But it may be a worthwhile expenditure for many computing applications. Considering the cost of the high-speed memory, several CPUs like the one described could be placed in parallel above the memory with little additional cost.

System interface. The optical computer based on the QWEST and integrated optics is especially well adapted to interfacing with other electronic and optical systems. The 10-micrometer infrared light can be coupled in and out directly with a coupler (see Figure 3d) with bandwidths of several terahertz. This light can be coupled to infrared fibers or imaged to arrays of detectors that create currents from the

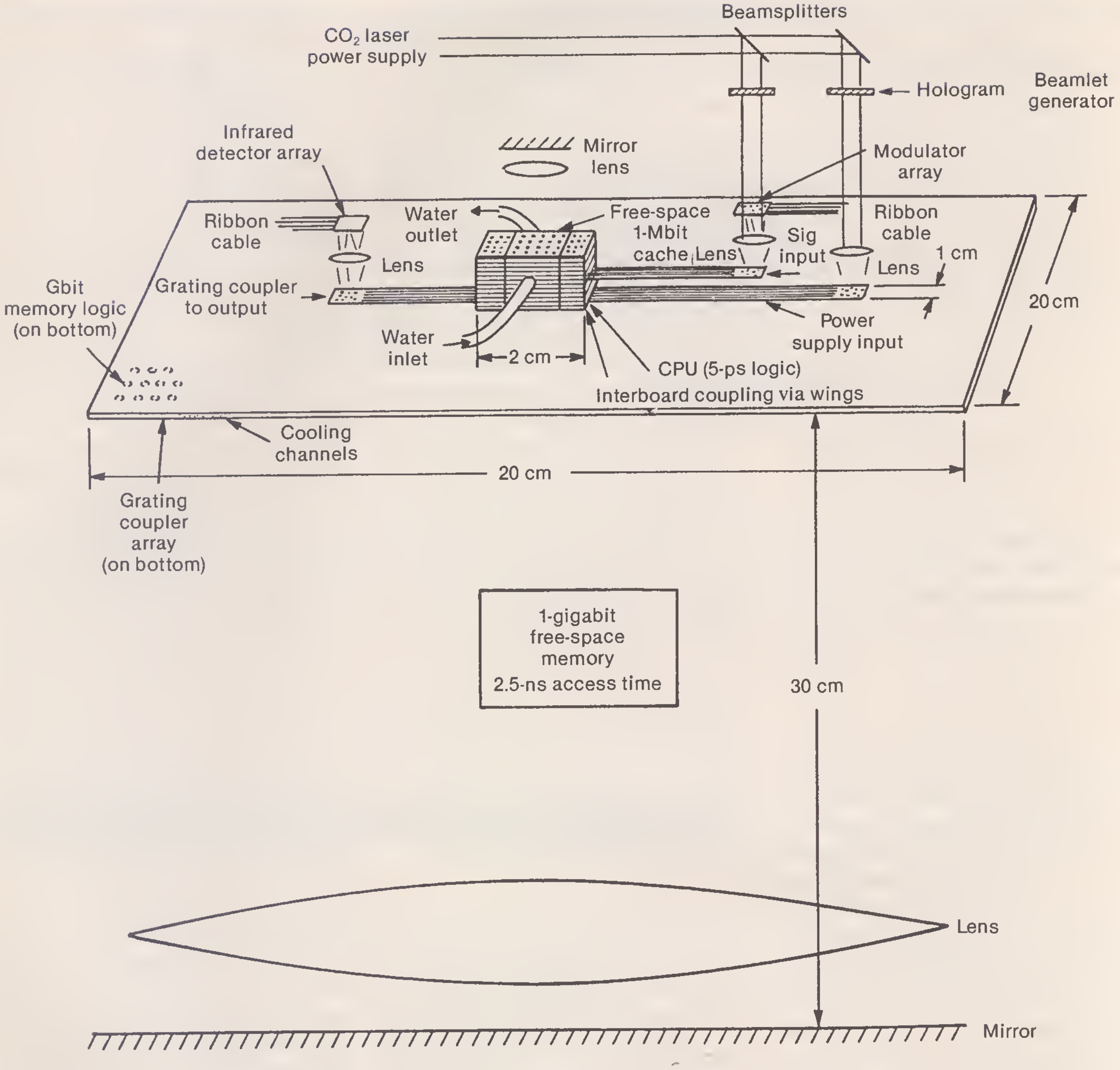

Figure 8. A conceptual computer system consisting of 40 boards of 10,000 logic gates apiece and a one-gigabit free-space memory. The worst-case propagation time across the CPU would be 150 picoseconds. The system is limited by size and propagation delays, so slower 5- to 10-picosecond logic is used in the CPU for power savings. The memory would be in free space with fast logic gates (one picosecond) maintaining the timing of the memory pulses and decoding the addresses. The interboard coupling is via grating couplers on the wings of each board. External connections for power, signals and rewire of engineering changes can be done by coupler boards inserted between the interboard couplers.

infrared light or modulators that create optical logic signals from electronic logic voltages.

A detector based on the QWEST transition with tunneling ionization from the upper level has been made with a responsivity of several amperes per watt and a speed suspected to be in the low picosecond range.[11] Similarly, we are working on the creation of a modulator with 100 to 1 contrast ratio with only a few volts applied to a subpicofarad capacitance device, also based on the QWEST transition. Thus, we believe it possible to directly connect with electronic logic systems at the tens of picosecond level.

Communications in optical fibers uses light with wavelengths from 0.9 to 1.5 micrometers. The QWEST can be created in all of the materials used in these systems. Direct modulation of the 0.9- to 1.5-micrometer light is possible with the 10-micrometer light since they both interact through the same lower quantum state of the conduction band. By filling or emptying this state, the 10-micrometer light could directly modulate the absorption at the other wavelength at picosecond speeds. The opposite effect can also occur. By using the 0.9- to 1.5-micrometer light to inject an electron into the lowest conduction band state from the valence band, the QWEST absorption at 10 micrometers can be modulated. The recovery time of this transition is relatively slow since it requires band-to-band relaxation. Via surface recombination, this time can be as fast as 20 picoseconds.

The integrated optical computer based on the QWEST promises to interface nicely, and directly, to either communication wavelength light or electronic logic-level voltages at high speed.

Cost. At this early stage, it's difficult to predict the cost of the optical computer. But with the larger powers of the first devices, one cost seems sure to dominate—that of the laser power supply. Assume pessimistically that the optical power required per 10-picosecond gate is 25 milliwatts. This assumed gate energy of 250 femtojoules is 10 times higher than that calculated previously, based on measurements of the QWEST optical properties.

A computer of 400,000 logic gates will need a laser power supply of about 10 kilowatts. A free-space gigabit memory with two-nanosecond access time needs a 100-kilowatt power supply. Today's large supercomputers use similar levels of power, but high-quality electronic power supplies cost about one to two dollars per watt, whereas lasers cost thousands of dollars per watt of high quality output. Even the diode laser is between \$1000 and \$10,000 per watt, if its price is divided by its small power output. An outstanding exception to the high laser cost is the CO_2 laser, which at the power levels of interest has an off-the-shelf cost of \$50 per watt of single-mode output.

The CO_2 laser offers some advantages: its output is tunable over a 9- to 11-micrometer range; it naturally becomes single mode, both transversely and longitudinally, because of the narrowness of each molecular line; and it has a wallplug efficiency of about 10 percent. Even this relatively economical CO_2 laser power supply will have a \$1 million to \$5 million price tag, depending on the fraction of a gigabit memory implemented.

With further improvements in the optical logic, the power per gate can be lowered a thousandfold before running into quantum statistical problems. The cost of the power supply would then drop to thousands of dollars, but other costs need consideration. Total wafer cost would be on the order of \$1000 for the full computer. Assembly and packaging of 40 nine-chip boards and associated interface chips would run in the low thousands as well. Because cost at this level involves numerous factors, many not related to actual construction of the computer, it is impossible to determine a price.

Power dissipation. The power is dissipated by cooling channels on the back of each board. Look first at the 10 kilowatts to be dissipated in the CPU. For 40 one-centimeter-square boards[3], we need to dissipate about 250 watts per square centimeter. Heat flux rates eight times higher than this have been demonstrated[12,13] with water cooling fins on the back of the substrate. The water needs to be pressurized to only 40 pounds per square inch, and it is inserted orthogonal to the side of the computer with the communication extensions (see Figure 7). The cooling fins are about 50 micrometers wide by 150 micrometers long with a 50-micrometer channel. The logic-gate temperature would rise 40 degrees Celsius above that of the cooling water, which could be near freezing. The logic gates should have a 150-degree operation range, giving good tolerance to this heating. Extension of this cooling to the memory is similar since the memory would have the same density of gates per area as the CPU.

Scaling. Developments toward faster computers will require smaller linewidths (for smaller computers) and faster logic gates. The material response currently indicates we could achieve gate delays down to the low hundreds of femtoseconds, including resonant build-up of the nonlinear field enhancements. The creation of a computer capable of using subpicosecond gates, however, will require submicrometer linewidths and millimeter-size instead of centimeter-size computers.

This scaling is possible. The QWEST can be built resonant with three-micrometer wavelengths, still using CO_2 lasers and doing the third harmonic conversion in the waveguides. Increased compactions and multilevel wiring could add the additional factor of three. But much below one picosecond, the computer will become more propagation-time limited, unless new architectures can efficiently expand the size of the computer usable for a given gate delay. The logic gate would need to be improved over the relatively crude logic gate described here, to lower laser cost and be compatible with lowered heat-removal techniques.

The first step toward a subpicosecond optical computer would be to lower the gate power to the quantum statistical level, or about 150 microwatts for a subpicosecond gate at the smaller three-micrometer wavelength. The nonlinear material only absorbs about 50 microwatts of this power. The remainder is transmitted or reflected by the Fabry-Perot cavity. One million of these gates would generate 50 watts of heat in the cubic-millimeter volume of the computer.

Without internal cooling channels, the temperature rise from center to surface could be less than 50 kelvin, assuming the thermal conductivity of GaAs. With copper cooling fingers occupying 30 percent of the volume, the temperature could be lowered another factor of three. With two or three levels of small cooling channels, the temperature rise could be made even smaller. As the QWEST appears to be tolerant to temperature changes over 200 K, much larger rises are tolerable. So, with cooling channels, compact one cubic millimeter operation may be possible with powers 10 to 30 times above the quantum limit, especially if a smaller fraction of the light is absorbed as heat. Note that superconducting devices are not tolerant to temperature rises of hundreds of kelvin.

Comparison with electronics. Speeds of current experimental electronic and optical logic devices, including how they function within systems, should be compared.

Electronic transistors have been tested in ring oscillators with speeds under 10 picoseconds, but an electronic logic gate in a system will be much slower because of increased fan-out and capacitance. Also the electronic wires have capacitance, inductance, and resistance. Superconducting transmission lines may eliminate the resistance but not the capacitance and inductance of these wires. Also, the creation of high-speed electronic transmission lines may involve complicated and expensive processing steps. The development of a 10-picosecond pin and compact packaging is required. The speed of an electronic system using these gates is still uncertain. An educated guess is that by the year 2000 electronic systems could effectively use 40-picosecond gates.[14]

In contrast, optical switching in a lab environment achieves speeds as fast as 0.01 picoseconds. The gates discussed here, which are more practical for system integration, are based on materials whose optical responses measure from 100 femtoseconds to as slow as 10 picoseconds, depending on use. Fabrication of the optical computer discussed here is based on the same GaAs quantum well technology as that of the fast electronic electronic logic being developed, but with higher speeds, room temperature operation, better immunity to impurities and defects, and larger two-micrometer linewidths.

Thus, optical logic can use many electronic developments, but with less-stringent requirements on fabrication results, environmental tolerance, and materials performance. Furthermore, system packaging of optical logic gates is simplified by the availability of compact surface-to-surface connectors with high-connection densities and multi-terahertz bandwidths. On these grounds, an optical computer based on the QWEST could be available sooner with higher performance than the electronic computer, since it uses a more primitive stage of the same development.

The only major independent development required is the new type of integrated optical elements. This development should be rapid, since it involves relatively simple thin-film deposition of optically transparent materials and their engineering into efficient elements with one-micrometer resolution lithography. With the development of this technology, medium integration density chips can be created, with interfacing to electronic logic, for special purpose applications. As the yields improve, gate powers lower, and gate densities increase, medium to large (1000 gate) chips can be integrated into a system.

Although the system discussed here is a relatively primitive first system, it will compete favorably with the best electronics has to offer by the turn of the century. But this system is only the starting point for optical logic. Normal engineering developments can push these systems to submillimeter size with gates in the 0.3- to 1-picosecond range, and other approaches can further extend the optical system. As logic signals approach 10-terahertz bandwidths, they are by definition approaching the infrared frequencies. It makes sense to begin development now of those technologies that handle the optical frequencies properly. ☐

Acknowledgments

Most of the concepts revealed here were developed as an employee at Lawrence Livermore National Laboratory and with the support of Lowell Wood. Further discussions of the waveguide and logic gate operation with Norm Whitaker have provided much insight into further improvements of the devices discussed. Also, I wish to acknowledge discussions with all members of the Optical Computing Department at Bell Labs.

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Reference number 10 (L.C. West, "Spectroscopy of GaAs Quantum Wells," PhD Thesis, Stanford University, July 1985) contains a large amount of unpublished information on the QWEST and is available free from the author. To request a copy, use number 180 on the Reader Service Card at the back of the magazine.

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Using Coincident Optical Pulses for Parallel Memory Addressing

Donald M. Chiarulli, Rami G. Melhem, and Steven P. Levitan
University of Pittsburgh

Common-bus, shared-memory multiprocessors are the most widely used parallel processing architectures. Unfortunately, these systems suffer from a memory/bus bandwidth limitation problem. For the designer of a hybrid optical/electronic supercomputer, an immediate temptation is to replace the shared electronic bus with an optical analog of higher bandwidth. To make that replacement is only a partial solution. The true bottleneck in such systems is in the address-decoding circuits of shared memory units.

In this article we propose a new memory structure that provides for parallel access in a multiprocessor environment. The proposed system has two advantages. First, it distributes the address-decoding circuitry to each of the requesting units on a common bus, thus eliminating the bottleneck of centralized decoding of encoded memory addresses. Second, it allows for parallel fetches of memory data with a level of parallelism limited only by the ratios of optical to electronic bus bandwidths and the dimensionality of the memory array.

By distributing the address-decoding function to the requesting units on an optical bus, this new memory structure eliminates the bottleneck of centralized decoding in multiprocessor environments.

In a conventional electronic memory circuit, like the one shown in Figure 1, an incoming memory address is divided into row and column addresses, each decoded separately. The selected memory location is the intersection of the select lines generated by the row and column decoders. In common-bus multiprocessors these decoders have traditionally been a performance-limiting bottleneck. Each decoder can process only a single encoded address, thus limiting memory access to a single location. Memory interleaving techniques,[1] which subdivide the memory space into regions, each in a separate memory unit, are commonly applied in an attempt to make parallel some subset of memory accesses. More recently, sophisticated cache memory systems,[2] which physically reproduce portions of shared memories in a local store, have been developed. Both systems have obvious limitations. Interleaved systems impose an ordering in which parallel accesses to a shared memory can be made, and cache memories rely on the locality of memory references for each processor and require a large overhead to support cache coherence.

Our solution is to distribute the address-decoding function to the requesting devices, thereby breaking contention for monolithic address decoders. This solution requires the abandonment of conventional encoded addresses as a mechanism for conserving bus bandwidth. Rather, we use the high bandwidth of optics to time-multiplex fully decoded addresses into an optical "select" pulse train. Using a technique based on the coincidence of optical pulses, we can directly apply the optical

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select pulse train to a memory array to address one or more cells. Effective parallelism is possible in this system because of the differential between optical and electronic bandwidths. Within a single electronic memory access cycle, N parallel memory references are possible, where N is limited only by the ratio of optical to electronic bandwidths. For a fixed bandwidth ratio the size of memory that can be constructed is further determined by the dimensionality of the memory structure. The technique requires no active optical or electro-optical switching devices. It uses only the mature technologies of optical sources, waveguides, and photodetectors. In the two-dimensional form, the system is well adapted to an integrated optics implementation.[3,4]

The addressing mechanism, which we call *optical pulse delay modulation*, is based on the use of time delays between optical pulses. The optical pulses are propagated through waveguides in several directions through the memory array. By appropriately adjusting the delays, we can make these pulses coincide at specific memory cells. This coincidence is detected by photodetectors at the addressed locations, thereby selecting those locations for memory access.

Our primary interest is in the application of this addressing mechanism to two-dimensional, multiported memory modules. Such structures are composed of horizontal and vertical waveguides with n memory cells located at the intersecting points. With proper cell layout we can access up to $\sqrt{n}$ memory cells concurrently by sending a sequence of pulses in the horizontal and vertical waveguides. In a multiprocessor environment a sequence of pulses, each corresponding to a distinct memory reference, is generated by independent address decoders located at each of the processing units. Thus, the address-decoding function is completely distributed to the requesting processors, and there is no address-decoding circuitry at the memory unit.

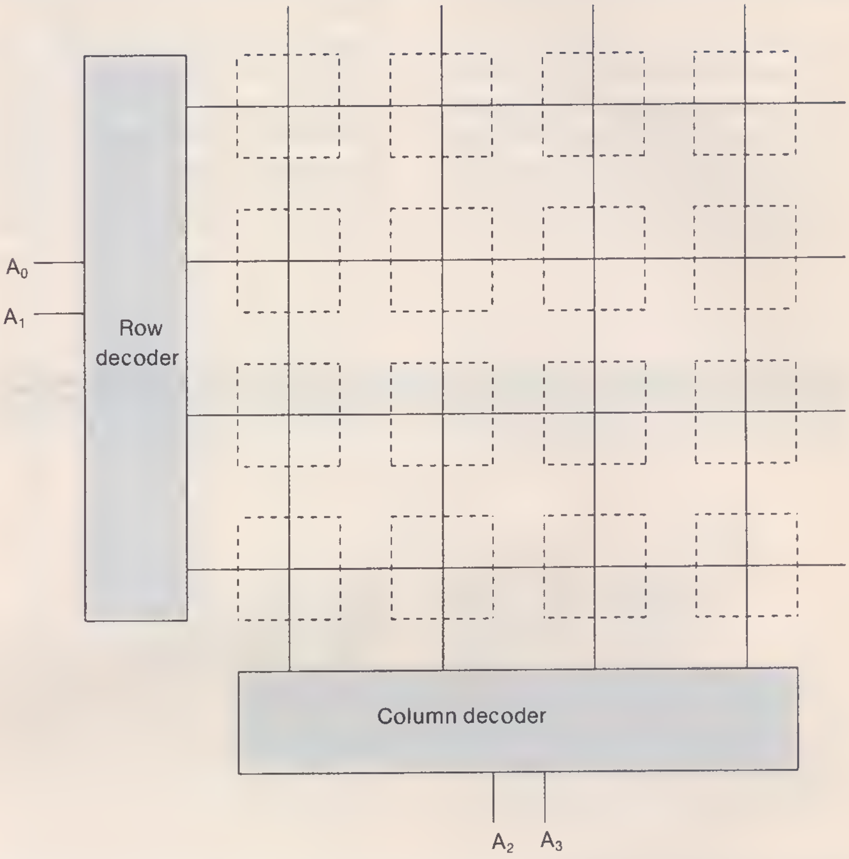

Figure 1. Conventional electronic memory structure.

A one-dimensional memory array

In this section we introduce the technique of pulse delay addressing, using a one-dimensional memory array as an example. This example is not ideal because both the hardware complexity and access time grow in proportion to the size of the memory. This is not the case for the higher-dimensional structures presented in later sections.

Optical pulse delay addressing. As shown in Figure 2, a memory module is composed of n cells $C_1, \ldots, C_n$, each storing one bit of information. The select signal for each cell C_k is an electronic pulse at the output of a photodetector D_k. The photodetector generates the logical OR of two incident optical signals, denoted in Figure 2 by s_1 and s_2.

The signals s_1 and s_2 travel in opposite directions along an optical path, which can be either an optical fiber or a planar waveguide in an integrated optical device.[5] Photodetectors are placed at fixed distance intervals d along the optical path, and two laser diodes, L_1 and L_2, are coupled to each end. Both laser diodes are normally *on* and the circuits of all detectors normally generate a logic *one*.

Assume that two dark pulses of duration τ are transmitted, one from L_1 and the other from L_2 at times t_1 and t_2, respectively. These pulses represent "dark spots" propagating at speed c_g (the speed of light in the waveguide). By carefully selecting the delay between t_1 and t_2, we can make the two dark spots meet at exactly one detector. This detector will then turn off, generating a logic *zero* of duration τ. The distance d between any two detectors is chosen to be equal to $d =$

τc_g, the propagation distance corresponding to the pulse duty cycle. The delay $t_1 - t_2$ is also chosen such that it is an even multiple of d. More specifically, if

$$t_1 - t_2 = (n - 1 - 2(k - 1))\tau \qquad (1)$$

then the two dark spots will meet at detector D_k, thus addressing cell k. For example, when $n = 5$, if L_2 generates its dark pulse 2τ seconds before L_1 generates its pulse, then Equation 1 gives $k = 2$; that is, the two pulses meet at D_2. Similarly, if L_2 generates its pulse 2τ seconds after L_1 generates its pulse, then the two pulses meet at D_4. Clearly, we choose the middle cell by generating the two pulses simultaneously—that is, by having $t_1 = t_2$. Therefore, the address of the cell is encoded by means of the delay $t_1 - t_2$. In this view, the pulse generated by L_1 may be defined as a reference pulse, and the pulse generated by L_2 becomes a select pulse. In the remaining discussion the terms t_{ref}, L_{ref}, t_{sel}, and L_{sel} will refer to t_1, L_1, t_2, and L_2, respectively.

The memory access time is determined by the maximum delay needed to address any cell in the array. From Equation 1, it is clear that for $k = 1, \ldots, n$, we have

$$-(n - 1)\tau \leq t_{ref} - t_{sel} \leq (n - 1)\tau \qquad (2a)$$

from which we find that the memory access time, σ, is given by

$$\sigma = 2n\tau \qquad (2b)$$

Note that Equation 2a indicates that the select pulse occurs within $n\tau$ before or after the reference pulse.

The parallelism in this addressing scheme comes from the fact that within time σ it is possible to address more than one cell by sending a series of pulses from L_{sel}, one for each memory reference. Each of these pulses will intersect with the reference pulse at the desired detector. In other words, parallel memory references are positionally distinguishable in a pulse train generated by a series of select pulses.

Before we describe how this memory can be incorporated into a shared-memory multiprocessor, two design issues at the interface between the electronic processing units and the optical system must be resolved. First, a system for generating a series of optical pulses corresponding to

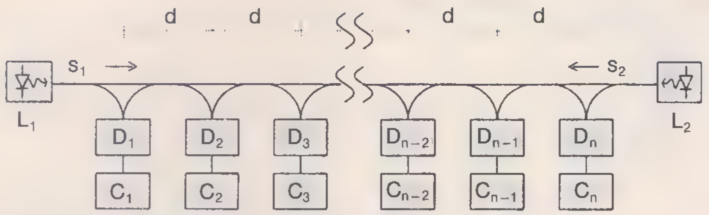

Figure 2. Linear memory structure.

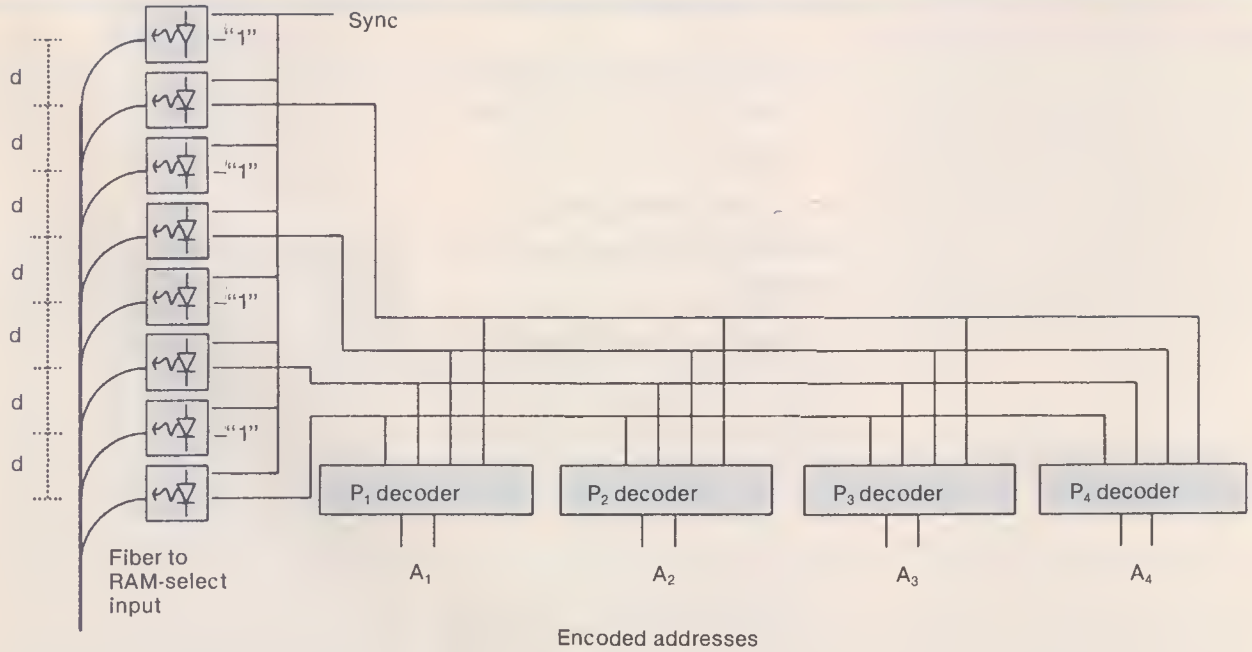

Figure 3. Distributed address generator.

the select pulse train must be specified. Second, the memory must allow data stored in the referenced locations to be returned to the requesting processors within a single processor memory cycle.

Address generation. One of the major advantages of the proposed memory organization over conventional systems is the removal of the address-decoding function from the memory unit and the distribution of this function to the requesting processors. More specifically, each of the processors is assumed to generate normal encoded addresses when referencing the shared memory. These addresses are decoded locally by an address decoder attached to each processor. The decoded addresses are electronically ORed onto a select bus common to all the processors. In the one-dimensional case the select bus consists of n lines, each controlling a laser diode pulser (see Figure 3). As will be explained later, the size of the select bus in the two-dimensional case reduces to a more manageable $2\sqrt{n}$ lines controlling $2\sqrt{n}$ laser diode pulsers.

Returning to the linear case, the optical pulse train containing the memory requests is generated by $2n$ laser diode pulsers spaced at incremental distances d in optical path length from the memory. To reconcile the difference between optical and electronic bandwidths, a single edge in the electronic time base (sync1 in Figure 3) controls the activation of all the pulsers such that all the optical pulses are generated simultaneously. If the duration of each optical pulse is equal to τ, then the select pulse train will be confined to $2n$ time slots, each with duration τ. Since proper time multiplexing of select pulses is not possible with the select pulsers constantly on, the n select pulsers connected to the electronic select bus are separated by n pulsers modulated by a fixed *one* signal (see Figure 3). Thus, all the slots will contain an optical pulse except those slots corresponding to requested memory addresses. More specifically, a dark spot (no pulse) at slot $2i-1$ corresponds to a request for memory location i.

In addition to the select pulse train, a dark reference pulse must be generated. Alternatively, the reference pulse is a series of $2n$ light pulses, with a single dark pulse at position n. Such a pulse train can be produced by a single laser diode that is normally *on* and is pulsed *off* for duration τ upon the reception of the synchronization pulse sync1. For the dark pulse in the reference train to coincide with pulse slot n in the select pulse train, the optical path from the reference diode to the memory should equal the optical path from the diode generating the middle pulse in the select train to the memory.

The above address generation scheme is crucially dependent on the simultaneous pulsing of several laser diodes. In an integrated optics environment, such synchronization problems can be avoided by the use of a single optical pulse source of duration τ and a series of electro-optic switches. In such an implementation each laser diode in Figure 3 is replaced by a directional coupler, which "couples in" the pulse at various optical path lengths. Synchronization problems are replaced in this system by a new set of issues relating to optical power distribution. We will discuss this and other issues relating to an integrated optics implementation in later sections.

Parallel memory read. The other issue at the interface between the electronic processing units and the optical system is a mechanism for returning the electronically stored data from the memory to the processors. The data is returned, on an optical bus, in a pulse train that consists of n slots, one for each memory location. Therefore, parallel accesses are positionally distinguishable in the read pulse train. When this pulse train arrives at a processor that has issued a read request for the ith position of the store, this processor will find the requested data in the ith slot of the data pulse train.

One method for generating the read data pulse train is to use a structure similar to the one depicted in Figure 4. In this structure, n laser diodes are placed on the optical data bus, separated by an optical distance d. When a specific memory location k is addressed, an electronic signal is generated from the photodetector as described earlier. The data at location k is assumed to be stored electronically and is used to modulate the kth laser diode only if location k is addressed. A synchronization signal, sync2, is used to synchronize the output of light (positive) pulses of duration τ from the selected memory locations that store a *one*. The difference in the optical path lengths between the laser diodes ensures the correct generation of the data pulse train. A similar technique, using detectors at fixed distances d and latching the pulse train at each processor interface, is used to demultiplex the pulse trains.

A two-dimensional memory structure

With the above mechanism it is possible to address all the n memory locations in one processor memory cycle. For the one-dimensional case this represents a sequential read of the entire store and requires a ratio of electronic to optical time bases equal to the size of the memory. Even for the most optimistic assumptions about achievable optical pulse widths, this structure will be inadequate and wasteful. However, applying a similar addressing mechanism to two-dimensional memory arrays reduces the required ratio of electronic to optical time bases to $\sqrt{n}$, where at

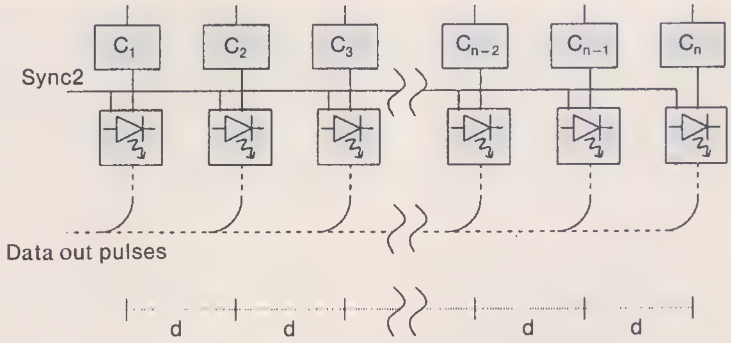

Figure 4. Generation of the data pulse train.

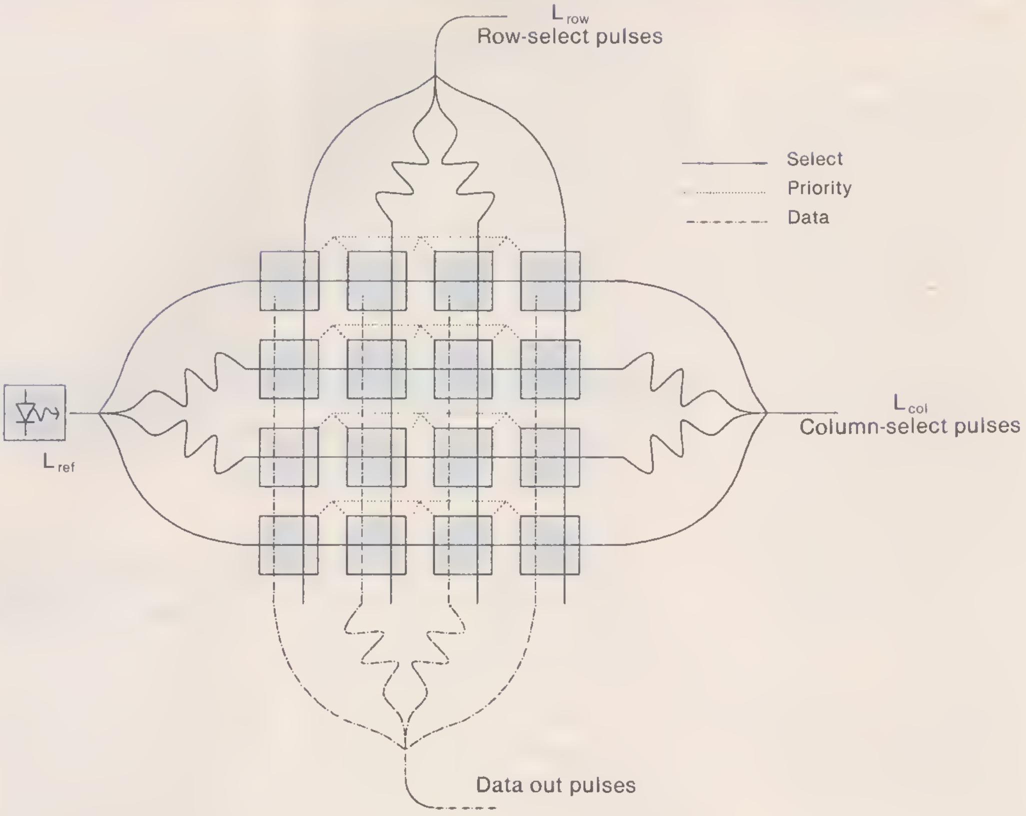

Figure 5. Two-dimensional memory structure.

most $\sqrt{n}$ memory locations can be addressed in one cycle. This allows for the construction of reasonable-size shared memories.

Coincident wavefront addressing. In the two-dimensional case we generalize the propagation of dark spots in one dimension to the propagation of linear dark wavefronts moving through a series of parallel waveguides. Hence, the method of addressing a location by programming the intersection of two dark spots can be generalized to addressing a location in a two-dimensional array by programming the intersection of three dark wavefronts. The literature on systolic and wavefront arrays (for example, H.T. Kung[6] and S.Y. Kung et al.[7]) suggests many possible ways for propagating and programming the intersection of wavefronts. Here we present a simple propagation scheme that can be used in two-dimensional memory addressing.

Consider two-dimensional memory arrays similar to the one shown in Figure 5. An array of size n is composed of $\sqrt{n} \times \sqrt{n}$ photodetector/cell units $DC_{i,j}$, $i,j = 1, \ldots, \sqrt{n}$, separated by a distance $d = \tau c_g$ in both the vertical and the horizontal directions. The structure of a DC unit is identical to the linear example, except that the input to the photodetector generates the logical OR of three optical signals: specifically, a dark reference wavefront generated by the reference diode L_{ref}, a select pulse train generated from a distributed set of column address decoders, L_{col}, both traveling horizontally in opposite directions, and a select pulse train generated by a distributed set of row select decoders, L_{row}, traveling vertically.

The optical signal generated by each source is decoupled from the source fiber by a "squid" connection into $\sqrt{n}$ signals that travel through the array in parallel waveguides. Since the optical path length of all legs in the squid will be equal, the wavefront will arrive at all locations in a single row (or column) simultaneously. For example, an optical pulse generated by L_{ref} and directed horizontally through the array will be simultaneously incident at locations $DC_{i,j}$, $i = 1, \ldots, \sqrt{n}$, in column j. Similarly, any pulse generated by L_{col} will arrive at all the cells in a specific column simultaneously, and any pulse generated by L_{row} will arrive at all the cells in a specific row simultaneously.

To derive the equations that govern the intersections of three wavefronts, assume, as in the case of the linear array, that all three laser diodes are *on* and that L_{ref} generates a dark pulse of duration τ at time t_{ref}. Also, L_{col} and L_{row} generate dark pulses at times t_{col} and t_{row}, respectively. If the timing of L_{col} is such that

$$t_{ref} - t_{col} = (\sqrt{n} - 1 - 2(j-1))\tau \qquad (3)$$

then the two dark wavefronts generated by L_{ref} and L_{col} will meet at column j of the array. To select a particular cell $DC_{i,j}$ in that column, the third dark wavefront, namely the one generated by L_{row}, should be crossing row i when the other two wavefronts meet at column j. This can be accomplished by timing L_{row} such that

$$t_{ref} - t_{row} = (j-i)\tau \qquad (4)$$

In other words, to address a certain memory location i,j, the column number j is encoded as $t_{ref} - t_{col}$, and the difference, $j-i$, between the column number and the row number is encoded as $t_{ref} - t_{row}$. From Equations 3 and 4 it can be shown that

$$-(\sqrt{n}-1)\tau \leq t_{ref} - t_{col} \leq (\sqrt{n}-1)\tau$$

and

$$-(\sqrt{n}-1)\tau \leq t_{ref} - t_{row} \leq (\sqrt{n}-1)\tau$$

and, hence, the memory access time, σ, is

$$\sigma = 2\sqrt{n}\tau \qquad (5)$$

As in the linear case, parallel accesses are made possible by the generation of multiple pulses in the row and column select signals. For example, Figure 6a shows the pulse trains for the selection of memory locations (2,2), (1,4), and (4,4) in the 16-location memory array of Figure 6b. For these three locations, $t_{ref} - t_{col}$ should equal -1, 3, and 3, respectively, and $t_{ref} - t_{row}$ should equal 0, 3, and 0, respectively. The locations of the wavefront resulting from these trains at times 0, 5τ, and 7τ are shown in Figures 6b, 6c, and 6d. It is clear from the intersection of the dark fronts in these figures that location (2,2) is selected at time 5τ and locations (1,4) and (4,4) are selected at time 7τ.

With the above scheme it is possible to encode the addresses of all the n memory cells in the column and row pulse trains during a single memory access cycle. However, for a time-multiplexed memory read such as the one proposed earlier, the length of the return data pulse train, and hence the total read time, would grow linearly with memory size. To prevent this and to facilitate a pipelined implementation, we chose the maximum length of the read pulse train to be $2\sqrt{n}$, the length of the select pulse trains. This is actually an advantage of the two-dimensional structure. More specifically, in the one-dimensional case, the memory cycle time was directly proportional to the size of the store. Each cycle needed to provide an optical time base slot for each location. In the two-dimensional case, access time and the possible number of parallel accesses are proportional to the square root of the number of locations in the store. This is a far more realistic scenario for constructing a shared-memory multiprocessor system. The price paid for this reduction in access time is the potential for conflicts in parallel memory accesses.

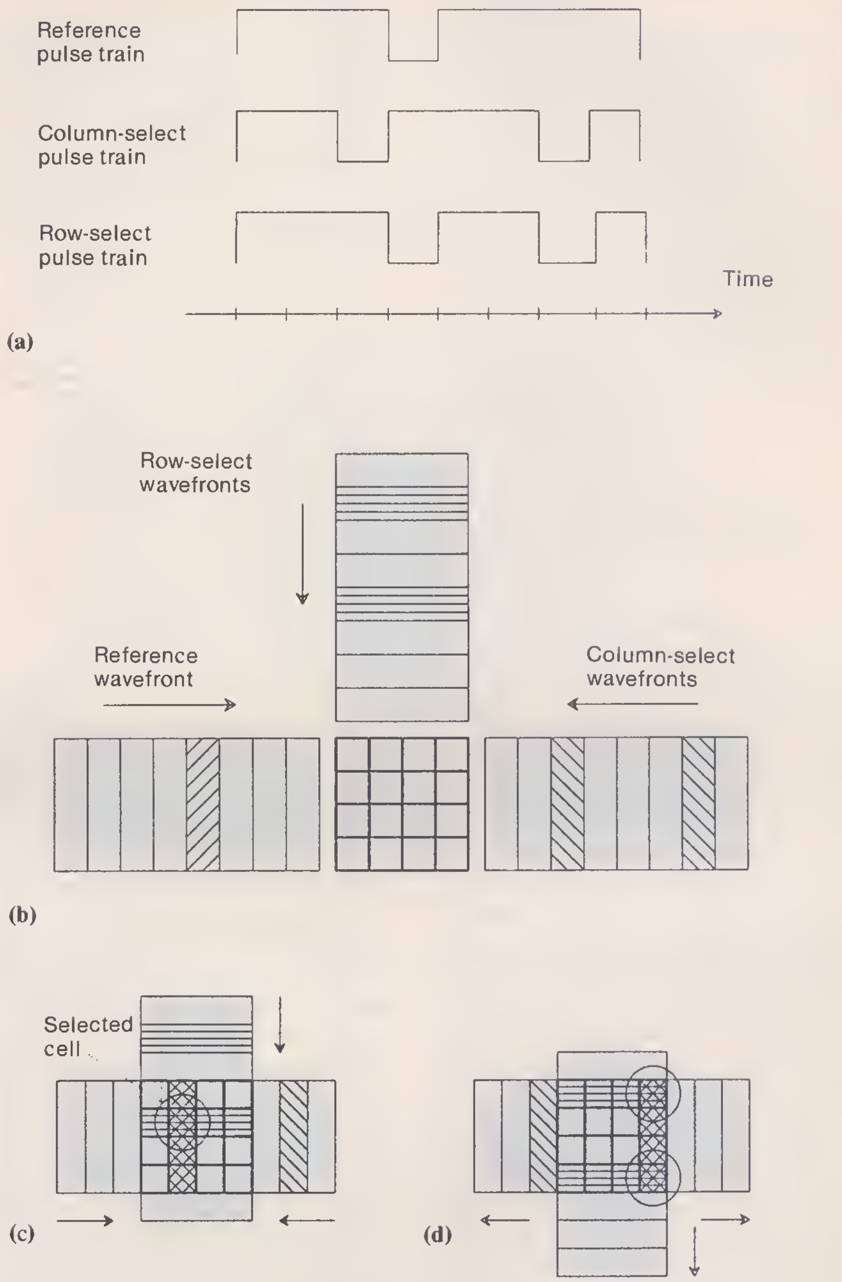

Figure 6. Programming the intersection of wavefronts, showing the select and reference pulse trains (a), the wavefronts at time 0 (b), and the wavefronts at times 5τ and 7τ (c and d).

Resolution of conflicts in memory access. Two policies can be applied to limit the number of memory references during a given cycle to $\sqrt{n}$. The first policy is to allow only $\sqrt{n}$ addresses to reach the memory module during the cycle, and the second is to allow as many as n addresses to reach the memory but return only the con-

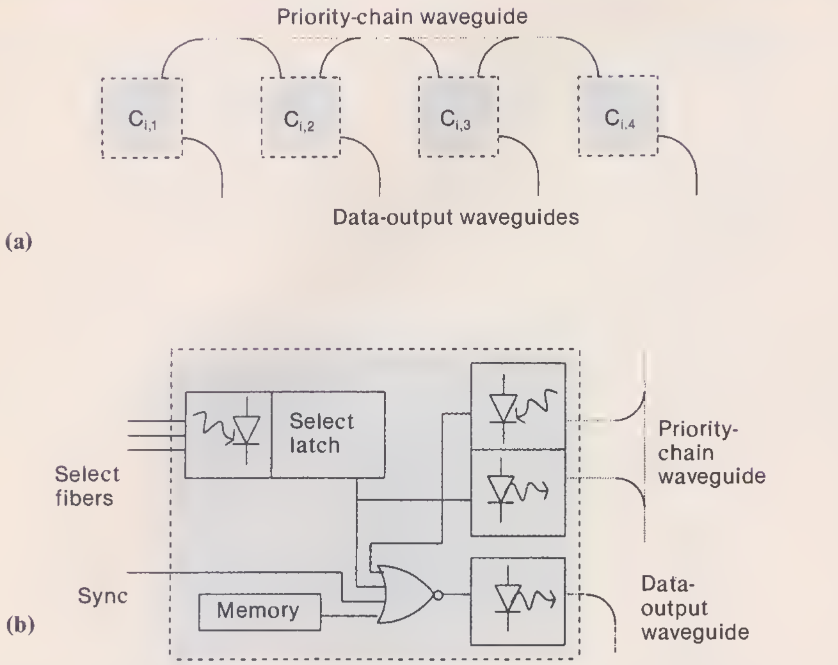

Figure 7. Conflict resolution strategy, with a prioritized memory row (a) and a typical memory cell (b).

tents of $\sqrt{n}$ of these addresses. The first policy requires active optical switching devices to resolve conflicts in the incoming select pulse trains. To avoid the need for such devices, we choose to implement the second policy, which allows full addressing and prioritizes referenced locations for conflict resolution.

The same data collection circuitry used in the linear array is used to collect data for each column of the two-dimensional array. One waveguide is dedicated to the collection of the contents of the addressed cells in each column. The signals in the $\sqrt{n}$ waveguides are merged into a single waveguide (denoted "dataout pulses" in Figure 5), which returns the data to the processors. The lengths of the waveguides are adjusted such that the optical paths between any two cells i,j and i,j' in the same row, i, and the merging point are equal.

With this collection mechanism, the content of any referenced cell i,j in column j will appear in the $(\sqrt{n}-i+1)$th time slot on the waveguide of column j. However, when the $\sqrt{n}$ pulse trains corresponding to the $\sqrt{n}$ columns are merged in the data output waveguide, the data produced by any two cells i,j and i,j' in the same row and different columns will collide. Since we have elected not to provide a mechanism for preventing conflicting addresses in the input pulse train, conflict resolution must be built into the memory array. That is, requests for memory references in the same row can be allowed, but only one request should be satisfied. Two problems arise for such a system. First, a mechanism to allow only one cell per row to output its data must be devised. Second, a method is needed for announcing which of the conflicting requests has been satisfied.

We start by resolving the second issue. The discussion to this point has assumed a single-bit memory. In fact, memory locations will contain an entire word of W bits, stored electronically and returned in parallel on W optical data out lines. If each memory location is tagged with its column number, then each processor can read the column address along with the data and use the data only if the address coincides with its request. If not, the processor must reissue the memory request. For a memory of size n, $\log(\sqrt{n})$ tag bits are needed, which increases the number of bits stored in each memory location from W to $W+\log(\sqrt{n})$.

The first of the conflict resolution issues is the more difficult. To prevent bus contention between conflicting requests, we have chosen a priority system based on an optical priority chain, like the one shown in Figure 7. Figure 7a shows a single row of a two-dimensional array. The optical distance from each cell in this row to the data output waveguide is equal, hence any parallel accesses within this row will conflict. To avoid this conflict, only one of the optical sources along this row can be allowed to generate data. The horizontal waveguide connecting all cells in the row forms an optical priority chain to resolve these conflicts.

Figure 7b shows a diagram of a typical memory cell. The optical OR output from the pulse-sensing photodetector sets the select latch. This output gates the contents of the memory cell through the three-input, electronic output control NOR gate. The third input to this NOR gate is the priority control. This signal is the output of a photodetector, which senses select signals for higher priority cells indicated optically on the priority chain waveguide. The local select signal is also used to turn on a laser diode, which injects light into the priority chain waveguide to indicate its selection to lower priority cells. Finally, the synchronization signal, sync2, ensures that all data out pulsers are activated simultaneously.

From the above description, it is clear that every memory read cycle is divided into three stages. In the first stage the select pulse trains are generated and propagated through the memory array. The minimum time required to complete this stage is equal to $2\sqrt{n}\tau$.

In the second stage the read operation is propagated through the memory cell electronics. Note that in Figure 5 the priority chain waveguides are parallel to the reference pulse waveguides. In this arrangement the wavefront that encodes current priority propagates through the priority chain waveguides during the first stage of the pipeline. The priority is delayed relative to the reference pulse by time

$$t_{pd} = t_s + t_l$$

where t_s is the switching delay of the detector/latch circuit and t_l is the turn-on time for the priority-out laser diode. At each cell in the rightmost column of Figure 5, which consists of the last cells to see the reference pulse and thus the lowest in the priority chain, the priority input signal arrives at the output control gate at time $t_{pd} + t_d$ relative to the arrival of the reference pulse (t_d is the response time of the priority-in detector). Since the select signal arrives at the output control gate in time t_s, the critical timing path for the second stage of the pipeline is

$$t_{pd} + t_d + t_g$$

where t_g is the output control gate switching time. By noting that t_l and t_d must be less than or equal to the pulse width τ, we can place the lower bound on second-stage pipeline delay at

$$t_s + t_g + \tau$$

Finally, in the third stage of the pipeline, data is returned from the memory to the requesting processors in a pulse train of $\sqrt{n}$ bits. Thus, the minimum time required for the third stage is $\sqrt{n}\tau$. Assuming that the memory size and the ratio of electronic to optical bandwidths is sufficient to satisfy

$$t_s + t_g < (2\sqrt{n} - 1)\tau$$

the longest of the stages is the first. With this three-stage pipeline the total memory cycle length is $6\sqrt{n}\tau$. Since we are accessing the memory in a pipelined fashion, and each stage can process $\sqrt{n}$ references, the effective memory bandwidth limit is $1/(2\tau)$ words per second.

Finally, we should mention that it is possible to support $2\sqrt{n}$ memory references per cycle, rather than merely $\sqrt{n}$, by rearranging the data collection waveguides of Figure 5. If the data collection waveguides are run diagonally, $2\sqrt{n}$ waveguides can be accommodated at the price of a more complex and unevenly distributed conflict resolution scheme.

Organization of memory modules. In the above discussion, we concentrated on select and read mechanisms, assuming a one-bit memory. In an $n \times W$-bit memory module we would reproduce W copies of the memory cell, the output control NOR gate, and the data output pulser of Figure 7b. For reading, only one decoder-select plane and one priority chain waveguide are necessary for each of the $W + \log(\sqrt{n})$-bit words in an n-word array. The only optical system that must be scaled with the number of bits in the word is the read output pulsers. In the same manner as an electronic memory, we must provide a separate return path for each bit.

Memory write control

For a conventional memory, support for write operations would require an additional control signal and a secondary data path for incoming data. Merely providing these additional signals in a parallel memory will not be adequate, since the issue of resolving mixed parallel reads and writes must also be resolved. The three possibilities for resolving this issue trade off write access time for optical circuit complexity:

(1) *Exclusive write:* In this solution we eliminate the possibility of mixed read/write operations and conflicting write operations. By implementing an external arbitration mechanism, we allow only exclusive write access to the memory. Once a single processor is selected, it can perform writes to the memory using conventional electronics. Although the system requires no additional optics, it results in nonparallel writes. If the ratio of writes to reads for the shared memory structure is relatively low, then exclusive write access represents a viable low-complexity alternative.

(2) *Full parallel read/write:* For full parallel optical writes it is not necessary to provide a separate optical write data bus. By combining control and data information in lieu of a data bus, we can provide fully parallel nonconflicting writes to any of the n locations in the store. In this technique each memory bit sees two bits of select information in each cycle—one bit from the read select optical circuit already described and a second from a *per-bit* local copy of that selection circuit used for write control. These two bits encode four states: read, write a zero, write a one, and do nothing (no select). Thus, by reproducing a second address selection structure at each bit in the word and by judiciously selecting code assignments for the four states, we limit the cost of this system to the addition of one optical selection plane for each bit.

This technique allows fully mixed reads and parallel writes. Any processor can write to any word with no conflict restrictions on the rows or columns of write addresses. However, there is no conflict resolution mechanism to prevent two processors from writing to the same address. As with a multiported electronic memory, such operations would generate unpredictable results. We assume that these mutual exclusion issues would be addressed by appropriate software.

(3) *Bit-serial parallel write:* At the cost of lengthening the overall write time, we can reduce the overhead for the full parallel read/write system to one additional optical selection plane by using a bit-serial approach. In this system a designated cycle initiates a W-bit serial write. The select signals generated by the read selection circuit during this cycle are latched separately and held for the duration of the serial write. Each subsequent cycle uses the write selection circuit to serially process each bit in the word. Meanwhile, parallel reads are still possible, concurrent with the serial write. A global counter/decoder circuit, to define the "current bit" as one of the W data bit planes of the memory, is necessary. It is the only additional overhead for this system.

Extensions and future research

We have concentrated in this presentation on the details of a two-dimensional memory array because of its suitability to integrated optical implementations. Nothing in the design prevents the linear wavefronts in two-dimensional arrays from being generalized to planar waves in three-dimensional arrays. In general, for m-dimensional memory arrays the access time is reduced to the mth root of the memory size. Hence, for a fixed bandwidth in the electronic system, the bandwidth requirements for the optical system are substantially reduced. This reduction is gained at the price of a corresponding reduction in the number of locations that can be referenced in parallel during a single electronic cycle. Like the access time, this number is also reduced to the mth root of the memory size.

Extensions of this technique can be applied to other two-dimensional switching structures. For example, the control information for a crossbar switch can be encoded into pulse trains and used to address specific switches in the crossbar. Pulse delay encoded control information can be prepended onto incoming packets to combine routing information and data without the need for optical-to-optical switching devices.

The question is: Can such a memory be built, and will its size and performance make it suitable for integration in computer systems of the next decade and beyond? The following issues must be examined:

(1) *Scalability:* The scale of the physical device is directly related to the optical pulse width. To minimize the physical spacing of detectors, very short pulses are required. For instance, reducing detector spacing to a scale that will allow monolithic integration will require picosecond pulse widths. Specifically, one-picosecond pulses will allow a detector spacing of 200 to 300 micrometers, depending on the refractive index of the optical medium. Current commercial technology for pulsing laser diodes in discrete devices provides for pulses on the order of 100 picoseconds. Recent research has produced optical pulses as short as eight femtoseconds.[8,9] In such research the common technique for pulse duration measurement is to split the pulse into two optical paths and detect coincidence when the paths are recombined at varying optical path lengths. On the basis of this trend we expect that the necessary pulse widths for an integrated optical implementation will be available in the near future. Meanwhile, we are currently using commercial discrete devices and optical fibers to examine scalability issues.

(2) *Detection limits:* A second limit on usable pulse duration is the detector technology for coincident light pulses. A two-dimensional memory requires that as many as three dark pulses are to be detected as they overlap. Even assuming the existence of photodetectors of sufficient bandwidth for single pulse detection, what degree of overlap is required to generate the optical OR of three pulses? Extended to multidimensional structures, fan-in limitations of this type become even more critical.

(3) *Fabrication versus physical limits:* As the system scales down in size and up in speed, what limits will be reached first—the fabrication limits of the technology or the physical limitations of the optical systems?

(4) *Clocking issues:* While there is little doubt that sufficiently narrow pulses can be generated by the electro-optics, the precision to which multiple pulses can be synchronized is an important question. Two coincident pulses must be timed to arrive with a precision of ±10 percent of their pulse width to allow for at least 80 percent overlap. This means that the electronic components must gate the optical signals with a constant delay that is precise to the optical time base. Clock distribution issues have been studied extensively in both electronic and optical domains. We believe that the required precision can be achieved by electronic circuitry. As an alternative, optical clock distribution techniques such as those proposed by Clymer and Goodman[10] can be applied.

(5) *Select latch response:* The electronic latches at the detector sites must respond to the selection pulses from optical detectors. These pulses will be no longer than the duration of the coincident pulses. This is a limitation on the speed of the optical system.

(6) *Waveguide decoupling technology:* In a two-dimensional design it is necessary to split incoming optical signals into parallel row and column waveguides. Detectors at each intersection must couple out sufficient optical power for detection, without significantly degrading the optical signal. Such highly asymmetric, single-mode directional couplers have been developed for optical fiber and are commercially available.[11] Several other techniques for low-power output coupling have been examined by Jackson et al.[12] Further work is needed to apply these techniques in an integrated optic environment.

In summary, we have presented a system that distributes the address-decoding function to the requesting units on an optical bus. In this system, addresses become optical pulse trains, and by arranging the optical paths, we provide a selection mechanism based on the coincidence of these pulses. In the coming year we plan to begin construction of a 64 × 16-bit register file based on this research, using discrete optical devices and fiber waveguides. This register file will be used as shared memory in a prototype eight-node multiprocessor. ☐

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Matrix Triangularization Using Arrays of Integrated Optical Givens Rotation Devices

Thomas K. Gaylord and Erik I. Verriest
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Solving linear equations is centrally important in many large-scale data processing problems. For example, problems such as weather prediction and the aerodynamic design of aircraft require repeated solution of the Navier-Stokes equation. The describing nonlinear systems of equations can be linearized at each time step to produce a linear system of equations that simplifies the problem-solving process.

In general, there are two approaches to solving sets of linear equations—direct methods and iterative methods. Perhaps the best known of the direct methods is Gaussian elimination. This method is generally sequential in nature. It also has the potential for being unstable: small errors in the intermediate steps may produce large errors in the final results. Iterative methods, on the other hand, are generally parallel and stable. However, they require an approximate matrix inverse as a starting point.

Optics-based devices and systems offer one means of solving sets of linear equations using a stable, direct method. These devices can employ Givens rotations[1] to perform matrix triangularization. In this article, we describe how to solve linear equations using an electro-optical system that employs arrays of optical Givens rotation devices. We examine how to implement this system using two different configurations, parallel and pipelined, and how to calibrate the system to minimize errors.

Integrated optical chips, implemented using waveguides and voltage-tunable diffraction gratings, can be used to solve sets of linear equations.

Attributes of optics

In telecommunications, fiber optics has played a dramatically increasing role in recent years. In addition, the role of guided wave optics (consisting of both fiber optics and integrated optical circuits) is expected to continue to grow at a rapid rate. This activity is largely oriented to switching networks. However, it will have a direct impact on signal and data processing as well.

The use of optics in computation is an exciting field offering great potential for large-scale, high-speed computing power. However, the nature of this potential must be well understood before it can be successfully utilized. The favorable and unfavorable characteristics of optics must be understood in relation to those of electronics so that overall optoelectronic systems can be designed to maximize the desirable features of each. Optics inherently has four powerful attributes:

- Large bandwidth. The high carrier frequency ($\approx 10^{14}$ Hz) offers the potential for very high speed operation. This attribute is primarily responsible for the success of fiber optics.
- Parallelism. Integrated optical (two-dimensional) and bulk optical (three-dimensional) systems are capable of handling and processing many channels of data simultaneously.
- Interconnectivity. In optical form, channels of data can physically pass

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through each other without altering the data. This property distinguishes optical signals significantly from the charge-based signals in metallic conductors, which must remain separate from each other. Interconnectivity allows the switching (interchanging or broadcasting) of data channels in any arbitrary pattern.

- Special functions. Numerous analytic functions can be implemented directly with optics. The best known of these is the Fourier transform, which gave rise to the field of "Fourier optics."[2] Other transforms (the Hadamard, the Hartley, the Mellin, the Radon, etc.) can also have direct optical implementations. Similarly, the sine and cosine can be implemented in optical form and are central to the type of processing described in this article.

A primary disadvantage of analog optics is low accuracy. This shortcoming makes these systems appropriate for fast, first-pass processors used in applications that do not require high accuracy. The attributes of optics thus differ dramatically from those of electronics. In general, a one-for-one substitution of optical devices for electronic devices in computing architectures should not be attempted. Such a strategy can be a fundamental mistake, as evidenced by some notable failures in the past.

Hybrid optical-electronic processing systems must efficiently use the inherent attributes of both optics and electronics in order to provide the advantage needed for large-scale complex processing problems. In this article, we describe a hybrid system that requires optical-electronic phase-sensitive detection and electronic feedback. Our discussion concentrates on the new technology involved in the optical component of this system.

The Givens rotation

The plane rotation operation for a rotation can be expressed as

$$\begin{bmatrix} y_1 \\ y_2 \end{bmatrix} = \begin{bmatrix} \cos\psi & -\sin\psi \\ \sin\psi & \cos\psi \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \qquad (1)$$

This equation can be written compactly as $\bar{y} = \mathbf{R}\bar{x}$, where the output vector $\bar{y} = [y_1, y_2]^T$, $\mathbf{R}$ is the rotation matrix, the input vector $\bar{x} = [x_1, x_2]^T$, and T denotes "transpose." (Throughout this article, a symbol in boldface type denotes a matrix.) The Givens orthogonalization[1] is obtained when $\sin\psi$ and $\cos\psi$ are found such that $y_1 = 0$. This operation can be used to make any specific element of a vector a zero. In fact, all but one entry of a vector can be zeroed by successive Givens rotations (involving different entries of the vector). For an $N \times N$ matrix, the triangularization process zeros all the elements above the diagonal (producing a lower triangular matrix $\mathbf{L}$) or zeros all the elements below the diagonal (producing an upper triangular matrix $\mathbf{U}$). The process of producing a lower triangular matrix for the case of $N = 5$ can be represented schematically as

$$\begin{bmatrix} a_{11} & a_{12} & a_{13} & a_{14} & a_{15} \\ a_{21} & a_{22} & a_{23} & a_{24} & a_{25} \\ a_{31} & a_{32} & a_{33} & a_{34} & a_{35} \\ a_{41} & a_{42} & a_{43} & a_{44} & a_{45} \\ a_{51} & a_{52} & a_{53} & a_{54} & a_{55} \end{bmatrix} \rightarrow \qquad (2)$$

$$\begin{bmatrix} b_{11} & 0 & 0 & 0 & 0 \\ b_{21} & b_{22} & 0 & 0 & 0 \\ b_{31} & b_{32} & b_{33} & 0 & 0 \\ b_{41} & b_{42} & b_{43} & b_{44} & 0 \\ b_{51} & b_{52} & b_{53} & b_{54} & b_{55} \end{bmatrix}$$

To start the process of lower matrix triangularization, $N-1$ rotations involving entries $i = 1, \ldots, N$ and $j = N$ are applied to transform the Nth column into the vector $[0, \ldots, 0, b_{NN}]^T$. The same rotations (in the same order) are used to transform columns 1 to $N-1$. The triangularization of the $N \times N$ matrix is accomplished recursively by zeroing the $N-1$ column of the resulting upper left $N-1 \times N-1$ submatrix, and so forth. Subsequent operations do not change the values in previously zeroed columns.

This algorithm lends itself naturally to cascaded or pipelined hardware implementations. Due to the nonlinear $\sin\psi$ and $\cos\psi$ functions, the Givens rotation operation consumes a significant amount of time and/or semiconductor material when implemented in digital electronics, even though efficient bit-recursive methods using simple shift and add operations known as coordinate rotation digital computing (Cordic) have been developed.[3]

Integrated optical Givens rotation device

The Givens rotation operation simulates a form of wave propagation and can be modeled as a lossless transmission line structure. Thus, wave propagation effects are a relevant design factor in the construction of this device. In a recent article, we reported on a coherent integrated optical implementation of an elementary rotation matrix device that operates on optical amplitude.[4] This device uses electro-optic grating diffraction and phase shifting to achieve the required sine evaluation, cosine evaluation, multiplications, addition, and subtraction in the Givens rotation operation.

The evaluation of sine and cosine is accomplished naturally and straightforwardly via diffraction by a thick transmission phase grating[5] induced by a voltage applied to periodic metallic electrodes on the surface of the device. The multiplication of the input amplitudes by the sine and cosine is accomplished as part of the diffraction process.

The summations in the Givens rotation are achieved by coherently combining the output waves from the grating. The phases of the waves are adjusted with electro-optic phase shifters to achieve the required addition and subtraction indicated in Equation 1. The subtraction process (for the y_1 output) is equivalent to coherent image subtraction. This operation may be performed using thick holograms and has been analyzed and experimentally demonstrated by Guest, Mirsalehi, and Gaylord.[6] The coherent addition process (for the y_2 output), likewise, is well established.

All of these functions can be combined into a single Givens rotation device as illustrated schematically in Figure 1a. A top view of an integrated optical implementation of this device is shown in Figure 1b. The optic axis is perpendicular to the surface. The crystalline material is Z-cut lithium niobate. The input light signals of amplitudes x_1 and x_2 are guided as transverse magnetic (TM) modes in channel waveguides ($\approx 8\ \mu$m wide). The interdigitated electrodes on this electro-optic material have a period, Λ, and an orientation such that the Bragg condition for diffraction is satisfied for both input waves for the freespace optical wavelength, λ. The angle of rotation, ψ, in Equation 1 is the grating strength parameter. It is proportional to the voltage, V_g, applied to the interdigitated electrodes and is given approximately by

$$\psi = [\pi d_g n_E^3 r_{33} V_g]/[\lambda\Lambda\cos(\alpha/2)] \qquad (3)$$

where d_g is the thickness of the grating, n_E is the index of refraction for the TM mode polarization, r_{33} is the electro-optic coefficient for this configuration, and α is the angle between the waveguides. One arm of the device contains electro-optic phase shifters to which static voltages are applied to produce the correct phase relationships between the input waves and between the output waves.[4]

This Givens rotation device is potentially simple to fabricate. It can be constructed by (1) fabricating (by diffusion or proton exchange) the channel waveguides, (2) growing a SiO_2 buffer layer over the surface, and (3) depositing the metal electrodes. In fact, this general type of device has been developed and fabricated for intensity modulation and switching applications[7,8] and recently analyzed for Givens rotation-type applications.[9]

Arrays of Givens rotation devices for matrix triangularization

In 1958, Givens[1] pointed out that plane rotations could be used to triangularize a matrix by applying elementary rotation operations repeatedly over pairs of ele-

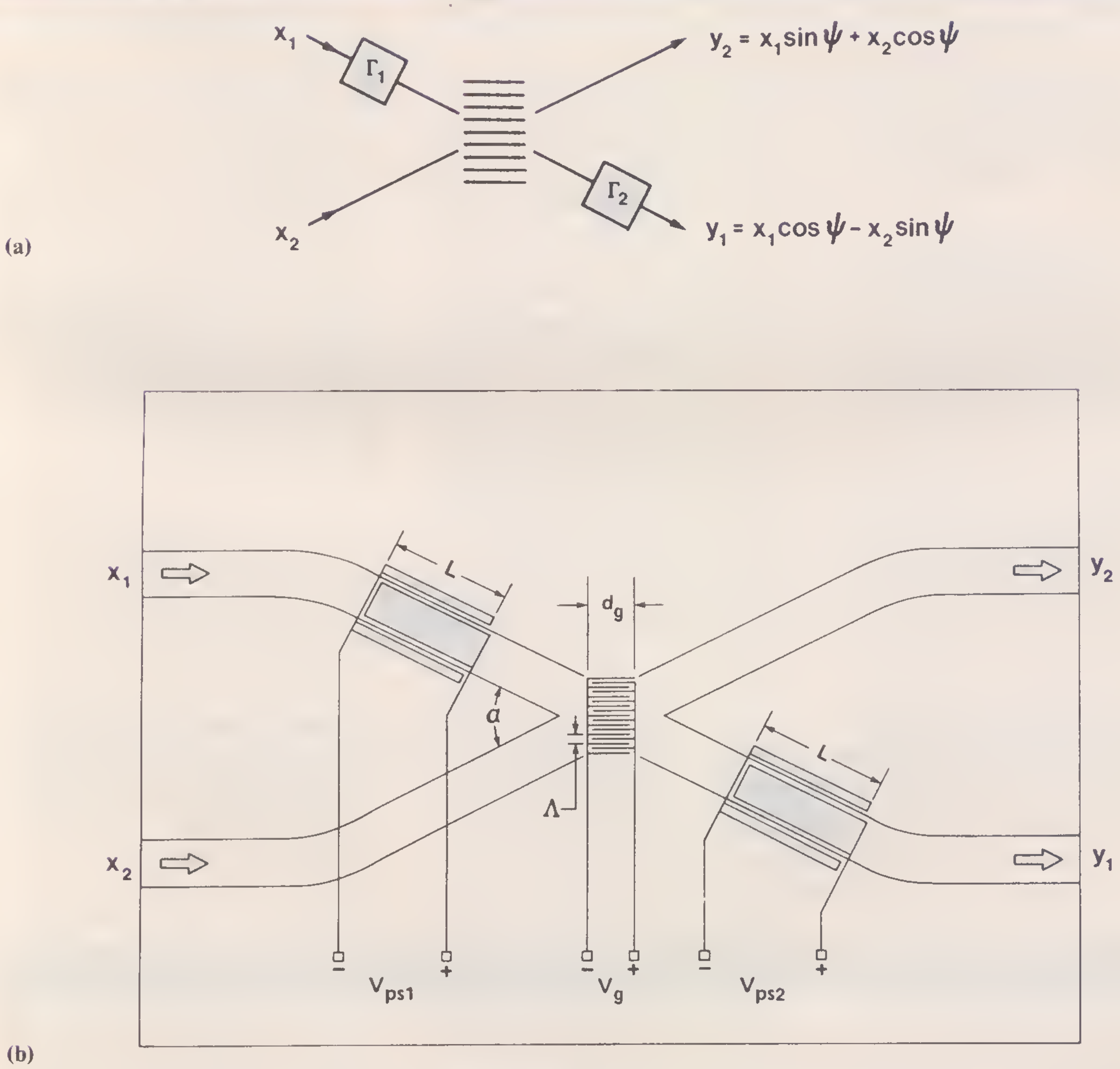

Figure 1. (a) The implementation of the elementary rotation operation. The optical input amplitudes x_1 and x_2 are diffracted by the thick grating and coherently combined to produce the output amplitudes y_1 and y_2. The external phase shifters (Γ_1 and Γ_2) have fixed values so that the transmitted and diffracted waves combine in phase (addition) for the y_2 output and combine 180 degrees out of phase (subtraction) for the y_1 output. (b) Schematic physical configuration of integrated optical elementary rotation device. A refractive index grating is formed at the intersection of the channel waveguides through the electro-optic effect by applying a voltage (V_g) to the interdigitated electrodes.

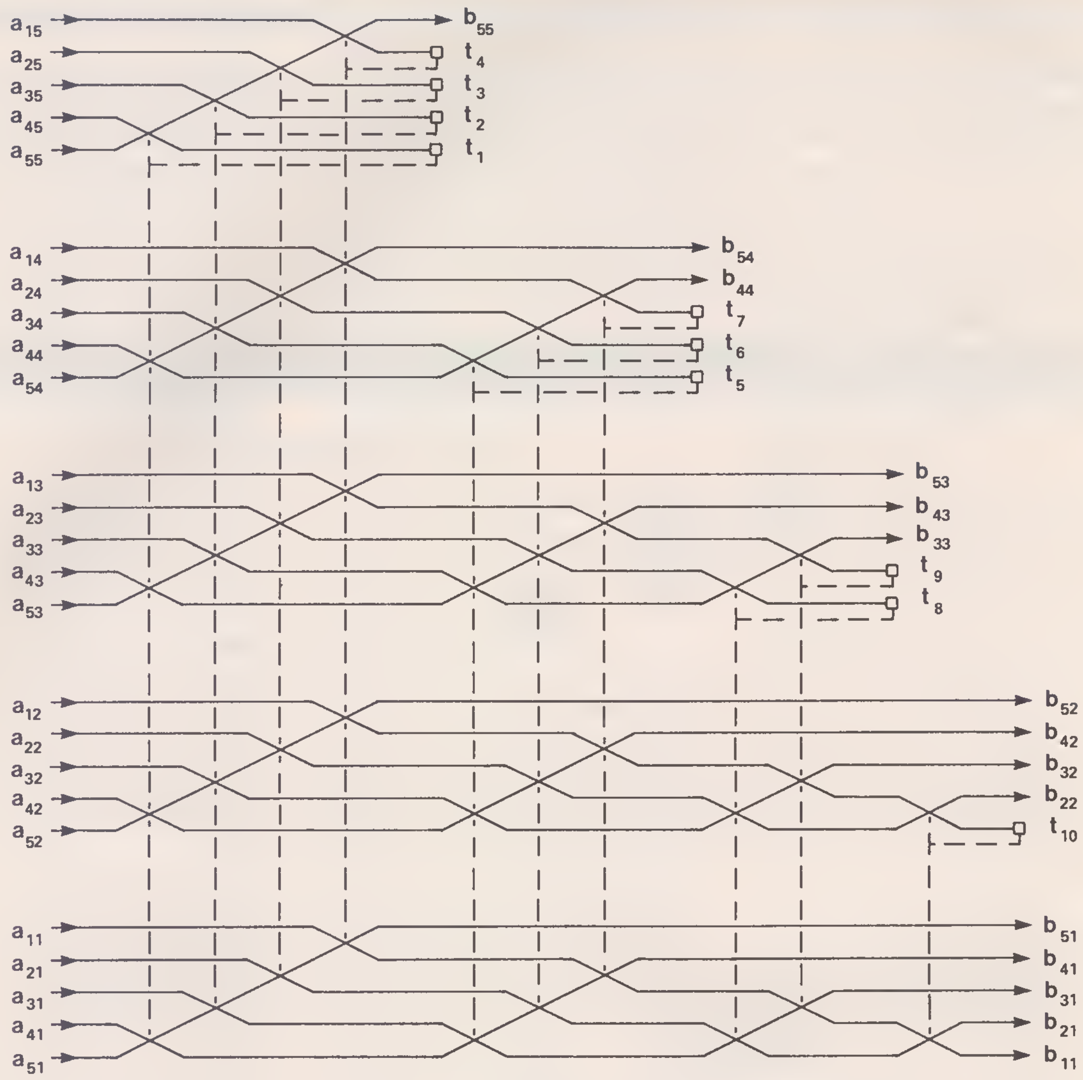

Figure 2. Parallel architecture for matrix triangularization. The solid lines are optical channel waveguides. A rotation device is located at each intersection of the channel waveguides. All rotation devices in a vertical column are electrically connected in parallel as indicated by the dashed lines. The squares represent photodetectors used to detect the nulling of matrix elements.

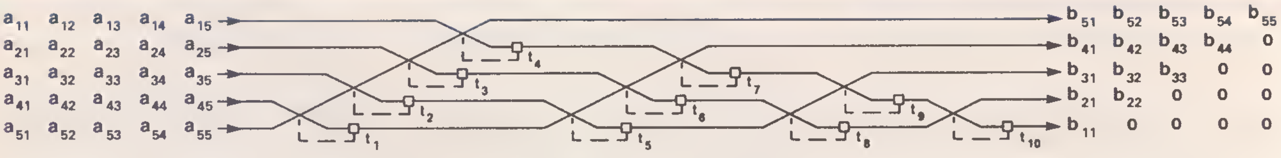
a_{11} a_{12} a_{13} a_{14} a_{15}
a_{21} a_{22} a_{23} a_{24} a_{25}
a_{31} a_{32} a_{33} a_{34} a_{35}
a_{41} a_{42} a_{43} a_{44} a_{45}
a_{51} a_{52} a_{53} a_{54} a_{55}
t_4
t_3
t_2
t_1
t_7
t_6
t_5
t_9
t_8
t_{10}
b_{51} b_{52} b_{53} b_{54} b_{55}
b_{41} b_{42} b_{43} b_{44} 0
b_{31} b_{32} b_{33} 0 0
b_{21} b_{22} 0 0 0
b_{11} 0 0 0 0

Figure 3. Pipelined architecture for matrix triangularization. The solid lines represent optical channel waveguides. A rotation device is located at each intersection of the channel waveguides. The squares represent photodetectors.

ments within the matrix. The integrated optical Givens rotation device described in the previous section has the capability of performing this operation. In principle, a single device could be used many times to accomplish the matrix triangularization. However, a more practical application is to integrate many Givens rotation devices on a single dielectric substrate in a manner analogous to integrating transistors on a single semiconductor substrate. Matrix triangularization can be accomplished by a parallel architecture or a pipelined architecture.

Figure 2 illustrates a parallel architecture implementation for the $N=5$ matrix triangularization that we used as an example above (see Equation 2). In this configuration, all N^2 matrix elements are entered into the system simultaneously. The solid lines in Figure 2 represent channel waveguides. At each intersection of channel waveguides is a rotation device as described in the previous section. Each dashed line represents a pair of metal conductors. All Givens rotation devices in a vertical column are connected together in parallel as shown. The optical amplitudes corresponding to the elements of the Nth column of the matrix enter the N channel waveguides at the top of the diagram. Detectors are represented by squares at the right. A detector at the end of each channel waveguide corresponds to matrix elements to be zeroed in the triangularization process.

The time steps associated with the triangularization process are labeled t_i (in this case, t_1 to t_{10}). In the first time interval, t_1, the value of $a_{4\,5}$ is initially detected (by the detector labeled t_1). The voltage applied to the leftmost column of rotators is swept until the amplitude detected is zero. This step zeros the $a_{4\,5}$ element and changes the $a_{5\,5}$ element according to Equation 1. Simultaneously, the elements a_{4j} and a_{5j} ($j=1$ to 4) are changed by the same rotation. The voltage on this column of rotators remains at this value for the remainder of the triangularization process. In the second time interval, t_2, the value of $a_{3\,5}$ is detected (by the detector labeled t_2). The voltage applied to the second column of rotators is swept until the detected amplitude of $a_{3\,5}$ is zero. The $a_{5\,5}$ element is correspondingly changed. At the same time, the elements a_{3j} and a_{5j} ($j=1$ to 4) are similarly transformed. After the time interval t_4, the fifth column has been entirely zeroed except for one element. This element has been transformed four times and is now $b_{5\,5}$, an element of the final triangularized matrix. All elements of the other columns experience the same transformations that zeroed the fifth column since the rotators in a vertical column are connected in parallel. In the fifth time interval, t_5, the new value of $a_{3\,4}$ is detected. The voltage applied to the fifth column of rotators is set so as to zero this amplitude. This step correspondingly changes the value of the $a_{4\,4}$ element and the other elements in this column of rotators. These operations continue through all time intervals. The output amplitudes shown in Figure 2 ($b_{1\,1}$ through $b_{5\,5}$) are the element values of the triangularized matrix. The total number of time steps and number of detectors is $(N^2-N)/2$. The total number of rotators required is $(N^3-N)/3$.

The $a_{i\,j}$ input elements and the $b_{i\,j}$ output elements may be positive or negative real numbers. The detected optical wave associated with a negative number is shifted in phase by 180 degrees relative to the phase of a positive number. Therefore, the values of the triangularized matrix must be detected using phase-sensitive techniques such as heterodyne or homodyne detection.[10] Thus the output amplitudes are detected in both magnitude and phase.

A pipelined architecture implementation for matrix triangularization using integrated optical Givens rotation devices is shown in Figure 3. Again, this architecture implements a triangular matrix of $N=5$. In this configuration, one column of N matrix elements is entered in parallel into the system. The optical amplitudes corresponding to the elements of the Nth column of the matrix enter first. This pipelined architecture includes a detector for each rotation device.

In the first time interval, t_1, the value of $a_{4\,5}$ is detected (by the detector labeled t_1) and the voltage applied to the first rotator is swept until the amplitude detected is zero. This step transforms the $a_{5\,5}$ element according to Equation 1. The voltage on this rotator remains at this value for the remainder of the triangularization process. Later, when the $N-1$ column arrives, the elements $a_{4\,4}$ and $a_{5\,4}$ are transformed by the same rotation. In the second time interval, t_2, the value of $a_{3\,5}$ is detected (by the detector labeled t_2). The voltage applied to this rotator is swept until the detected amplitude is zero. This step changes the $a_{5\,5}$ element correspondingly. After the time interval t_4, the fifth column has been entirely zeroed except for the $b_{5\,5}$ element of the final triangularized matrix. One after another, the elements of the other columns experience the same transformations that zeroed the fifth column. It experiences no further changes as shown by the straight section of waveguide in Figure 3. In the fifth time interval, t_5, the new value of $a_{3\,4}$ is detected. The voltage applied to this rotator is set so as to zero this amplitude. The value of $a_{4\,4}$ is correspondingly transformed. This mode of operation continues. Finally, the first column enters and experiences all of the previously set rotations. The output amplitudes shown ($b_{1\,1}$ through $b_{5\,5}$) are the element values of the triangularized matrix.

The total number of time steps is $(N^2+N-2)/2$. The number of detectors is again $(N^2-N)/2$. The total number of rotators required is $(N^2-N)/2$, making the pipelined architecture a more practical configuration than the parallel architecture. However, the stricter timing and the required delays create more complexity for signal flow control.

Inaccuracies, detection, and calibration

In the above discussion, we have described the transformation produced by the ideal Givens rotation. In practice, a variety of errors are possible during device operation. First, errors may be induced by inaccuracies in the construction of the device. Second, errors may be induced by inaccurate control settings (the voltages applied to the interdigitated electrodes and to the phase shifters). Third, at the detection stage, inaccuracies may occur due to the shot noise in the optical signal and thermal noise in the electronic amplifiers following the detectors. The first two types of errors can be minimized by proper calibration before operation. In fact, the values of the needed rotation angles are "hidden variables": their values are not explicitly required if the devices are used in an adaptive mode such as that of the architectures described in the previous section.

An analysis of the device physics reveals several possible deviations from the desired rotation transformation matrix given in Equation 1. The bends in the waveguides may produce small losses. Any deviation from the design value in the angle between the crossing waveguides may induce crosstalk between the channels. Such losses result in an additional rotation, small losses, and phase shifts in the beams. Inaccuracies in the device parameters and small drifts in the operating frequencies induce further deviations in the grating strength as given by Equation 3. These produce a further additive component in the rotation angle. As a result, the actual transformation matrix before calibration is not given by Equation 1, but in phasor notation by

$$\exp(j\Gamma_0)\begin{bmatrix}\sigma_1\exp(j\Gamma_2) & 0\\ 0 & \sigma_2\end{bmatrix}\cdot \begin{bmatrix}\cos\psi & \exp(j\zeta_a)\sin\psi\\ \exp(j\zeta_b)\sin\psi & \cos\psi\end{bmatrix}\cdot \begin{bmatrix}\sigma_3\exp(j\Gamma_1) & 0\\ 0 & \sigma_4\end{bmatrix} \quad (4)$$

where Γ_0 is the overall phase shift of the output with respect to the local oscillator (in the detection process), σ's are attenuation coefficients, Γ_1 and Γ_2 are each a tunable phase shift plus a phase shift due to inaccuracies, ζ_a and ζ_b are phase shifts inherent in the diffraction process,[9] and ψ is the grating strength parameter. The attenuations are typically very small, so the attenuation coefficients can be given as $\sigma_i = 1-\gamma_i^2$ with $\gamma_i \ll 1$. The grating strength parameter is $\psi = KV_g$, where V_g is the voltage applied to the interdigitated electrodes and K is an effective gain. The controllable parameters are V_g and Γ_i. As shown below, the calibration procedure can eliminate most of the errors by a suitable choice of V_g and Γ_i. However, small inaccuracies may still exist. These persistent errors occur because the calibration procedure (in the same manner as the system operation) involves detection of the output.

The coherent detection in the present case is like that commonly used in coherent fiber-optic communication systems. A received signal amplitude is coherently added with a stronger signal from a local oscillator (a reference beam). The combined optical signal impinges on a photodiode. In homodyne detection, the signal and the reference beam have the same wavelength. Two photodiodes are used to establish a balanced detection scheme. One receives the sum signal and the other the difference signal. To obtain the sum and difference signals, the beams (typically with a 90 degree angle between them) intersect at a beamsplitter (each beam having a 45 degree angle of incidence). For amplitudes of the transmitted reference and signal beams measuring A_R and A_S respectively and a relative phase shift between the beams of Γ_0, the difference of the photo detector currents Δi is[11]

$$\Delta i = (2\eta q\lambda/\mathrm{hc})A_R A_S\cos\Gamma_0 \quad (5)$$

where η is the photodetector quantum efficiency, q is the electronic charge, λ is the wavelength, h is Planck's constant, and c is the speed of light.

Inaccuracies may occur at the detection stage due to the quantization of the optical field. These inaccuracies are equivalent to the presence of noise usually called "shot noise," which is a manifestation of the discrete nature of photons.[11] Noise also occurs as thermal noise in the electronic amplifiers. Cooling the amplifiers minimizes the latter. Integration of the signal in time also decreases these uncertainties, but at the expense of slower system operation. The shot noise increases with local oscillator power level, so that if the reference amplitude is made sufficiently large, the thermal component becomes negligible. The shot-noise-limited signal-to-noise ratio (achievable, for instance, with a low capacitance p-i-n diode followed by a microwave field-effect transistor amplifier) is[11]

$$SNR = (2\eta\lambda/B\mathrm{hc})A_S^2\cos^2\Gamma_0 \quad (6)$$

where B is the bandwidth of the detector. The overall effect is that a signal amplitude A (in phase with the reference beam) is detected as $A+\sigma\varepsilon$, where ε can be modeled as a standard normally distributed error with variance $\sigma^2 = 2[B\mathrm{k}T + (\eta\lambda/B\mathrm{hc})]/\tau$, where T is the absolute temperature, k is Boltzmann's constant, and τ is the integration time of the detector amplifier.

Calibration before operation eliminates most of these errors. This procedure uses relatively long integration times and slowly ramped voltages to eliminate noise effects. The calibration procedure has three steps. For the first two steps, the x_2 input amplitude (see Equation 4) is set to unity and the x_1 amplitude to zero. In this case, the detectable output signals $\hat{y}_1$ and $\hat{y}_2$ are

$$\hat{y}_1 = \sigma_1\sigma_4\cos(\Gamma_0+\Gamma_2+\zeta_a)\sin\psi$$

and (7)

$$\hat{y}_2 = \sigma_2\sigma_4\cos\Gamma_0\cos\psi$$

First, the grating voltage V_g is applied so that the detected signal $\hat{y}_1$ is zero. The phase shift Γ_0 is adjusted so that the detected signal $\hat{y}_2$ is maximum. The product $\sigma_2\sigma_4$ is measured. Second, using the same configuration, V_g is tuned so that $\hat{y}_2$ is zero, and Γ_2 is adjusted to maximize $\hat{y}_1$. The product $\sigma_1\sigma_4$ is measured. Third, keeping a fixed voltage applied to the grating, the first input beam is set to unity and the second input beam to zero. Now the detectable signals are

$$\hat{y}_1 = 0$$

and (8)

$$\hat{y}_2 = \sigma_2\sigma_3(\Gamma_1+\zeta_b)$$

The phase shift Γ_1 is adjusted to maximize the detected signal $\hat{y}_2$. The system is now calibrated. A small error remains due to the residual individually unadjustable attenuation factors σ_i. Therefore, with system calibration, the rotation transformation matrix is

$$\begin{bmatrix}\sigma_1 & 0\\ 0 & \sigma_2\end{bmatrix}\begin{bmatrix}\cos\psi & -\sin\psi\\ \sin\psi & \cos\psi\end{bmatrix}\begin{bmatrix}\sigma_3 & 0\\ 0 & \sigma_4\end{bmatrix} \quad (9)$$

Tuning the gains in the detection amplifiers compensates for the effects of some of the products of σ_i. For one device, this procedure only gives two degrees of freedom. Fortunately, with proper fabrication these attenuations can be very small. (For example, Becker and Johnson recently reported a loss of 0.08 decibel per one degree bend.[12])

Processor accuracy

The accuracy of this type of matrix triangularization processor is an issue of fundamental importance. In this section, we evaluate accuracy in three stages. First, we examine the accuracy in one elementary rotation transformation. Second, we examine the process of nulling all but one element of a given N-dimensional vector. Third, we assess the accuracy of the solution of a set of linear equations using the pipelined matrix triangularization architecture in a hybrid configuration that employs backsubstitution.

Accuracy of the elementary rotation transformation. In operation, the integration time of the detector amplifier is not as large as during calibration. If a rotation is to null the element y_1 in Equation 1, the actual detection will terminate when the signal plus noise are zero ($\hat{y}_1 = 0$). The nonzero y_2 output also contains noise. The detected output $\hat{y}_2$ is described by

$$\begin{bmatrix}0\\ \hat{y}_2\end{bmatrix} = \begin{bmatrix}\cos\psi & -\sin\psi\\ \sin\psi & \cos\psi\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}e_1\\ e_2\end{bmatrix} \quad (10)$$

The two detector noises, e_1 and e_2, are independent and identically distributed. The correct rotation angle ψ must satisfy $\tan\psi = x_1/x_2$. However, the actual rotation angle produced in the presence of the noise is $\psi' = \psi - \sin^{-1}[e_1/(x_1^2 + x_2^2)^{1/2}]$, where it is assumed that the total signal power in the vector $\overline{x}$ far exceeds the noise power. Letting $r_{i,j}$ equal $(x_i^2 + x_j^2)^{1/2}$ and using $1/\varrho$ for the ratio of the standard deviation σ of the independent identically distributed errors to $r_{1,2}$, we can write the actual angle of rotation as $\psi' = \psi - \sin^{-1}(\varepsilon_1/\varrho)$, where $e_1 = \sigma\varepsilon_1$, and ε_1 is modeled by a standard Gaussian distribution. The small noise assumption corresponds to $\varrho \gg 1$. As noted earlier, this rotation angle is not explicitly needed.

The detected output signal $\hat{y}_2$ is also a random variable given by $\hat{y}_2 = e_2 + (x_1^2 + x_2^2 - e_1^2)^{1/2} \approx \sigma\varepsilon_2 + r_{1,2}(1 - \varepsilon_1^2/2\varrho^2)$. Using the same low noise approximation, the average value of the detected output is

$$<\hat{y}_2> = r_{1,2}(1 - 1/2\varrho^2) \tag{11}$$

The average output $<\hat{y}_2>$ is the norm of the vector $[x_1, x_2]^T$ as computed optically. It contains bias. The normalized variance in this quantity is $\sigma^2(1 + 1/2\varrho^2)$, assuming a Gaussian distribution. Note that these error statistics are the same if the $\hat{y}_2$ is zeroed, and the norm of $\hat{y}_1$ is detected. The attenuations left after calibration are negligible compared to the detector-induced errors.

Accuracy of zeroing all of the elements but one in an *N*-dimensional vector. In the pipelined implementation shown in Figure 3, zeroing all of the elements but one in a column is equivalent to computing the norm of an N-dimensional vector. Detection of the output signal $\hat{b}_N$ (the norm of the Nth column vector) occurs after $N-1$ rotation steps. An error is introduced at detector t_1 as the a_{N-1} component of the vector is zeroed. The first resultant signal, $\hat{b}_{N,1}$ (a "partial" norm), at the upper output branch of this rotation device is then $\hat{b}_{N,1} = r_{N,N-1}(1 - e_1^2/r_{N,N-1}^2)^{1/2}$. Since this signal does not need to be detected, there is no additional noise except for that induced by the nulling method. This relation can be rewritten $\hat{b}_{N,1}^2 = a_{N-1}^2 + a_N^2 - e_1^2$. Proceeding diagonally along the pipeline, an additional error e_2 is introduced, giving a second resultant signal of $\hat{b}_{N,2}^2 = a_{N-2}^2 + a_{N-1}^2 + a_N^2 - e_1^2 - e_2^2$. Iterating through $N-1$ steps and adding the final detection error e_N yields the detected norm $\hat{b}_N$ for the entire Nth column of

$$\hat{b}_N = b_N[1 - \sum_{i=1}^{N-1} (e_i/\varrho)^2]^{1/2} + e_N \tag{12}$$

The quantity ϱ for this case is b_N/σ, where b_N is the exact norm of the vector. The average value is $<\hat{b}_N> = b_N[1 - (N-1)/2\sigma^2]$ with variance $\sigma^2[1 + (N-1)/2\varrho^2]$. In the presence of noise, the process of zeroing all of the elements but one in a column vector of length N can be expressed as

$$\begin{bmatrix} 0 \\ \cdot \\ \cdot \\ \cdot \\ 0 \\ \hat{b}_N \end{bmatrix} = \begin{bmatrix} \\ \quad R_N \quad \\ \\ \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \\ \cdot \\ \cdot \\ \cdot \\ a_N \end{bmatrix} + \begin{bmatrix} e_1 \\ e_2 \\ \cdot \\ \cdot \\ \cdot \\ e_N \end{bmatrix} \tag{13}$$

where R_N is the overall orthogonal column transformation that has produced the detected output vector $[0, \ldots, 0, \hat{b}_N]^T$.

Accuracy of linear equation solving via triangularization. A nested series of the orthogonal column transformations described by Equation 13 is needed to analyze the accuracy in triangularizing a matrix. After $N-1$ sets of rotation devices, a lower triangular matrix of processed elements is produced together with independent and identically distributed error elements in the upper triangular portion of the matrix. This process can be represented by

$$\{R_2 \cdots R_{N-1} R_N\}A = \left[\begin{array}{ccc} \diagdown & & E_U \\ & \diagdown & \\ L & & \diagdown \end{array}\right] \tag{14}$$

where **L** represents the processed elements in the triangularized matrix and $\mathbf{E}_U$ represents the errors in the upper portion of the matrix. Detection of the processed elements in **L** adds another lower triangular matrix $\mathbf{E}_L$ of independent and identically distributed detection errors.

The solution of the system of equations $\overline{v} = \mathbf{A}\overline{u}$ proceeds by entering the columns of the **A** matrix followed by $\overline{v}$, the vector of constants. If the resulting matrix were perfectly triangular, the solution for $\overline{u}$ would follow easily by backsubstitution. However, only a perturbed version of the lower triangular matrix $\{\mathbf{R}_2 \ldots \mathbf{R}_{N-1}\mathbf{R}_N\}\mathbf{A}\overline{u}$ and the processed $\overline{v}$ elements, namely $\{\mathbf{R}_2 \ldots \mathbf{R}_{N-1}\mathbf{R}_N\}\overline{v}$, are available for detection. From these values, electronic backsubstitution can proceed to obtain a solution. The solution vector $\hat{u}$ is described by $(\mathbf{L} + \mathbf{E}_L)\hat{u} = \{\mathbf{R}_2 \ldots \mathbf{R}_{N-1}\mathbf{R}_N\}\overline{v} + \overline{e}_v$, where $\overline{e}_v$ and $\mathbf{E}_L$ are respectively a vector and an upper triangular matrix of independent and identically distributed errors introduced in the detection process. The computed solution vector $\hat{u}$ can be expressed to first-order in terms of the exact solution vector $\overline{u}$ as

$$\hat{u} = \overline{u} + \mathbf{L}^{-1}(\overline{e}_v + \mathbf{E}\overline{u}) \tag{15}$$

where $\mathbf{E} = \mathbf{E}_U - \mathbf{E}_L$. For a single pipeline, the errors $\mathbf{E}_L$, $\mathbf{E}_U$, and **E** are all fixed by the initial triangularization process. Therefore, averaging over $\overline{e}$ reveals a bias. The ensemble average over numerous pipelines solving the same problem is zero with a corresponding covariance matrix of $\sigma^2(1 + \|\overline{u}\|^2)\mathbf{A}^{-1}\mathbf{A}^{-T}$, where $\|\overline{u}\|$ is the norm of $\overline{u}$ and $\mathbf{L}^{-1}\mathbf{L}^{-T}$ is approximated by $\mathbf{A}^{-1}\mathbf{A}^{-T}$. It is possible to eliminate this bias by iterating alternately between an optical pipeline and an electronic processor (performing only additions and multiplications). Thus a processing system solving the same problem repetitively converges to a statistical steady state whose average is the exact solution $\overline{u}$.

The arrays of Givens rotation devices that we have described utilize several of the favorable attributes of optics. They utilize parallelism (in one dimension) by allowing a simultaneous input into arrays of devices. They utilize interconnectivity by the intersection and modification of the channels of data. Finally, they utilize the special functions capability of optics by evaluating sine and cosine directly (without the use of a sequential algorithm).

Beyond solving sets of linear equations, matrix triangularization can be used to implement various square-root algorithms (in Kalman filtering and solving the Lyapunov and Riccati equations). Furthermore, a form of the lattice (or ladder) filter structure, described by the square-root-normalized lattice equations, has a natural interpretation in terms of rotations. These structures can also be implemented with arrays of other types of integrated optical devices.[13] Lattice filters are widely used for prediction and filtering in the areas of speech processing, channel equalization, seismic data interpretation, and electroencephalogram (EEG) analysis. This range of possible uses suggests that arrays of integrated optical Givens rotation devices may have many applications in the future, not only in solving sets of linear equations, but also in performing other critical signal-processing functions. ☐

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Optical Bistability, Logic Gating, and Waveguide Operation in Semiconductor Etalons

M.E. Warren, S.W. Koch, and H.M. Gibbs
University of Arizona

Semiconductor etalons have potential application as all-optical logic devices both for parallel-processing systems and for integrated optical circuits compatible with fiber-optic data transmission.

As more and more of the information essential to our society travels in the form of light signals, present computer architectures and IC technology impose limitations on the computational power needed to deal with that information.[1] Consequently, interest has developed in performing more of the processing of this data optically. There are now many research groups in the US and abroad, including university-industry cooperative research centers funded by the National Science Foundation and cooperating companies, working in the general area of optical signal processing, parallel processing, and computing. The major advantages of optics for data-processing applications are its parallelism, bandwidth, and potentially large interconnection capability. To utilize these advantages, one needs optical devices suitable for integration and new system architectures.

A fundamental component needed for a computing or information-processing system utilizing light as the information-carrying medium is the optical analog of the digital logic gate. This is a device in which single or multiple optical inputs can result in one of two output states, which in turn can serve as inputs to further devices. Nonlinear Fabry-Perot etalons are one candidate for such applications. They are capable of exhibiting optical bistability under suitable operating conditions. Bistability is defined as the existence of two output states for the same input value over some range of input values. Even though optical bistability is not a necessary property for such applications, an optically bistable device can be operated as an optical logic gate or as a switching device. (A recent monograph by Gibbs presents a thorough treatment of the development of optical bistability and its applications, as well as an extensive bibliography.[2])

This article describes the application of one type of optical bistable device based on gallium arsenide as the nonlinear medium. We discuss several possible operations with GaAs nonlinear Fabry-Perot etalons. Rather than summarizing the large number of experimental results with these devices, this article utilizes a recently developed computer model to illustrate the basic operating principles and applications. The architecture and systems issues of optical computing are not the focus of this article, since we mainly concentrate on the device operation itself. In keeping with common practice we will use the term *optical bistable device* when referring to a device that can exhibit optical bistability even when not being used in such a manner. Instead of the expression *nonlinear Fabry-Perot etalon,* we will often use *nonlinear etalons* or *etalon devices*.

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The nonlinear Fabry-Perot etalon

The basic concept behind nonlinear etalon devices is the Fabry-Perot interferometer. This device consists of two partially reflecting mirrors separated by a distance L, as shown in Figure 1. The arrangement is essentially that of a resonant cavity. The light sent into the cavity undergoes multiple reflections at the mirrors, and interference occurs between the forward and backward traveling partial field components. At the same time, the light inside the cavity suffers some losses due to diffraction, transmission through the mirrors, and absorption in the material filling the space between the mirrors. If the light inside the cavity is sufficiently coherent, the interference between the counter-propagating beams can lead to dramatic modifications of the intensity at different wavelengths. If the light wavelength is such that an integral number of half waves will exactly span the distance between the mirrors, the interference is constructive. Consequently, the intensity in the cavity is very high and the transmission through the etalon can be very large—close to 100 percent if the losses are small. If, on the other hand, the light wavelength is not in resonance with the cavity length, destructive interference occurs in the cavity, the intracavity intensity is low, and a low transmission state of the device is realized.

To make an etalon device whose performance utilizes a nonlinear dependence on the light intensity, it is necessary to fill the space between the mirrors with a material that has intensity-dependent optical properties. In other words, the etalon absorption or the index of refraction must vary with the intensity of the exciting light. If the absorption is a function of the light intensity inside the cavity in such a way that its value decreases with increasing intensity, the material is called a *saturable absorber*. In this case the quality of the etalon will increase sharply with increasing intensity so that an initially opaque device can "switch on" to a highly transmitting state. In so-called dispersive devices the refractive index of the medium depends on changes in the light intensity, which cause the optical path between the mirrors of the etalon to change. This effect tunes the etalon in or out of resonance with light of a fixed wavelength. Absorptive and dispersive changes usually occur simultaneously, but either may be dominant in a particular wavelength regime.

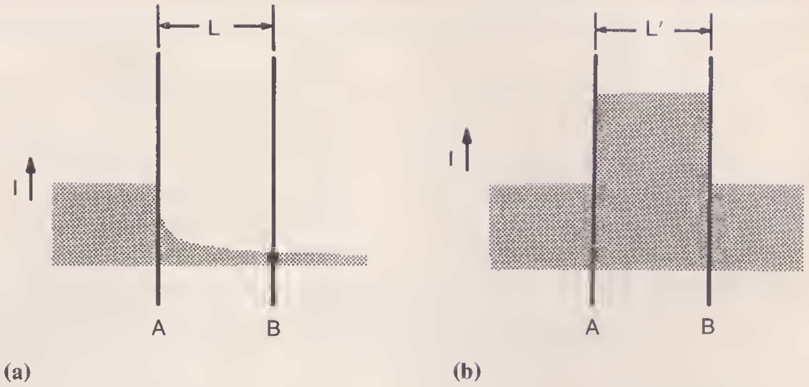


Figure 1. Schematic of Fabry-Perot etalon: in (a), separation L, between mirrors A and B, is not an integer number of half wavelengths (negative feedback); in (b), the separation L' is an integer number of half wavelengths (positive feedback). The shaded regions represent the relative light intensities before, after, and inside the etalon.

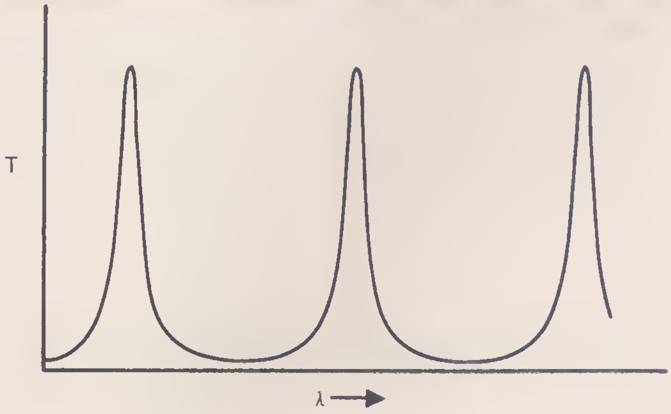


Figure 2. Transmission of a Fabry-Perot etalon as a function of the light wavelength, with high-transmission peaks for wavelengths in resonance with the cavity.

Figure 2 shows the transmission of a Fabry-Perot etalon as a function of the light wavelength. One sees a series of high-transmission peaks occurring at regular intervals where the wavelength satisfies the resonance condition mentioned earlier. If the etalon contains a material whose main nonlinearity is the index of refraction, the

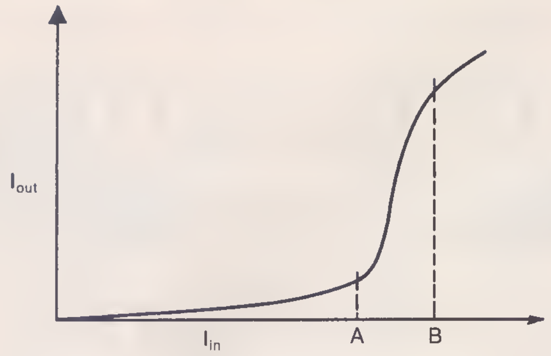


Figure 3. A representative plot of output intensity versus input intensity for a nonlinear Fabry-Perot etalon that does not exhibit bistability. The etalon is initially not in resonance with the light and is tuned into resonance with increasing intensity, so that the etalon becomes highly transmitting. If the etalon is biased by a beam of intensity A, an additional intensity of $B-A$ is sufficient to switch the device to high transmission.

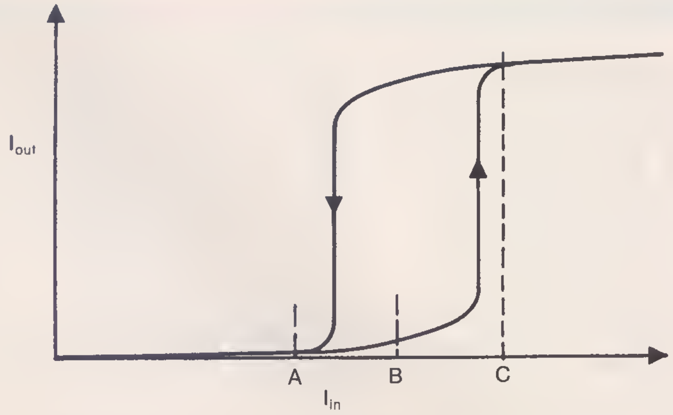


Figure 4. A representative plot of output intensity versus input intensity for a bistable Fabry-Perot etalon. The arrows indicate the curves followed when the device has increasing input intensity (switch-up) and decreasing input intensity (switch-down).

transmission peaks will move with varying intensity relative to the wavelength scale. A particular transmission peak may be shifted toward or away from a fixed laser wavelength (the operating wavelength). A nonlinear etalon that initially is not in resonance (or is "detuned" from resonance) may very well be quite opaque originally, but it can switch to a highly transmitting state as the light intensity increases. Conversely, if the light is initially in resonance, the device may switch to a low-transmission state as the intensity is changed. These dispersive nonlinear etalons can operate efficiently with low loss, making them the most interesting etalon device for logic and switching applications.

The attractiveness of nonlinear etalons is increased by the fact that the reflected light from the front surface shows nonlinear behavior complementary to the transmitted light. Therefore, one can utilize both reflected and transmitted signals. In proposed applications of such devices, the intensity dependence is used for the logic operations and the wavelength of the light is held constant, or sometimes two discrete wavelengths are applied (see the "Optical logic gates" section). However, in any such applications the input and output signals from the device are of the same form: light intensity values. This is an important attribute for practical system applications. There is no need for external nonoptical power sources or addressing mechanisms for these devices.

Figures 3 and 4 illustrate two typical intensity responses of a nonlinear Fabry-Perot etalon that can be realized in the same device by slightly changing the operating wavelength (i.e., the detuning from the resonance). In both cases the transmission is a strongly nonlinear function of the incident intensity, but in Figure 3 a monostable situation is depicted, whereas bistability is depicted in Figure 4. Bistability can be achieved only if the material nonlinearity and the feedback from the etalon's mirrors are sufficient. The effect is best illustrated as a hysteresis loop for a situation in which a pulse incident on the device has rising and falling edges varying linearly in time (a triangular pulse). Hysteresis loops are obtained from the actual input and output pulses by plotting output intensity versus input intensity at any instant of time. The hysteresis loop in Figure 4 is characteristic of a mostly dispersive nonlinear material where the output intensity exhibits strong saturation behavior for input intensities above the switch-on value. In the case of a saturable absorber mentioned earlier, the transmitted intensity after switch-on varies almost linearly with the incident intensity because the switching has been achieved by bleaching the material.

The nonlinear but monostable response characteristics shown in Figure 3 serve as a simple example of an optical logic gate. If the total light intensity on the device is the value at point A, the transmission is low. If additional light signals bring the total incident light intensity to point B, the device becomes highly transmitting. This type of response can be regarded as a logic gate if one applies a bias beam and normalizes the signal beams to represent logical values of 1. Using the characteristics of Figure 3, one can realize both AND and OR gates, depending on the magnitude of the bias beam, which can be adjusted to determine whether the system requires one or two signal beams to increase the intensity from A to B. Negating functions can be performed in reflection, and more complex logic operations are possible if more than one light wavelength is used.

Nonlinear semiconductor materials

The choice of the nonlinear medium is the most important determinant of the properties and performance of an optical logic device. A material that shows a large nonlinear change in its index of refraction is the preferred choice because of the flexibility of devices based on dispersive tuning of the etalon. The size of the nonlinearity regulates the power requirements for device operation—a critical issue with proposed all-optical logic devices. Ideally, the material would also be nearly transparent at its operating wavelength or at least have a readily saturable absorption in order to reduce absorptive losses. Moreover, the material nonlinearities should respond very quickly to the changes of incident light intensity to allow high-speed operation.

To date, direct-gap semiconductors are the best materials known for nonlinear optics applications that combine the need for large nonlinearities, fast switching, sophisticated fabrication technology, and good material quality in terms of purity and quality of surfaces. Nevertheless, the search for other materials or more refined material structures is a very important research effort in the semiconductor and nonlinear optics area. By now, the effect of optical bistability has been demonstrated with a large variety of semiconductor materials; GaAs,[3] cadmium sulfide (CdS),[4] indium antimonide (InSb), and zinc selenide (ZnSe)[5] are just a few examples. Although we concentrate in this article on devices based on room temperature bulk GaAs, which certainly is one of the most promising materials to date, the basic principles we describe here are also valid for the other materials.

Extensive experimental and theoretical work in GaAs nonlinear optical devices has been in progress for more than a decade. To understand the origin of the optical nonlinearities in the wavelength region of the fundamental semiconductor absorption edge, one has to investigate the coupling between the semiconductor material and the light field. In direct-gap semiconductors the absorption of photons excites electrons from the valence band into the conduction band. The missing electrons in the valence band are called *holes*. Both conduction band electrons and valence band holes are quantum mechanical excitations that are not attributed to any particular atom in the material but are "collective excitations" of the entire crystal. Electrons and holes can be regarded as elementary quasiparticles that have a mass defined by the band structure, an electrical charge, and a spin. Their electrical charges are of opposite sign, since the hole has the charge of the completely filled valence band minus one electron. As charged quasiparticles, conduction band electrons and valence band holes interact through the Coulomb potential. This interaction causes a strong correlation between electrons and holes and may even lead to the formation of bound states (excitons), which may be regarded as hydrogen-atom-like quasiparticles characterized by a Bohr radius and a binding energy.

All these different quasiparticles have only a finite lifetime, which varies from several hundred picoseconds to several nanoseconds in most direct-gap semiconductors. This lifetime is a consequence of the fact that electrons and holes may recombine radiatively or nonradiatively. The recombination is the opposite effect of electron hole creation. In the case of radiative recombination the energy stored in the electron hole pairs is emitted as photons, whereas nonradiative recombination occurs if the energy is transferred to other elementary excitations such as lattice vibrations or to impurities.

Laser excitation of semiconductor materials creates a particular density of electrons and holes, which constitute a quantum mechanical many-body system. The various interaction processes among these elementary excitations strongly modify the optical properties of the crystal. One important nonlinearity is caused by the fact that no two electrons (or holes) can be in the same quantum state. Consequently, electrons and holes fill up their bands, thereby blocking future transitions into the same states. A blocked transition is not able to absorb any additional photons, showing up in the spectra as a saturation of the absorption. At the same time, other optical nonlinearities are introduced through many-body effects such as screening of the Coulomb interaction or reduction of the bandgap. The resulting changes of the semiconductor absorption and dispersion depend on the density of excited electron hole pairs and therefore on the intensity of the exciting laser light. Since there has to be some absorption in the material to produce the excited charge carriers, a fundamental trade-off between the requirements of high transparency and large nonlinearity must be considered in any device operation. The best one can hope for is an absorption that can be readily saturated so that large index effects are produced and the excited semiconductor becomes more transparent.

A consistent description of the nonlinear optical properties of semiconductors requires a quantum mechanical calculation of the material absorption and refractive index spectra by means of modern many-body techniques.[6] Since this article is not the place to discuss any details of these theoretical attempts, we only want to show some results of our recent calculations for GaAs. We used the so-called plasma theory[7] to generate values for the absorption and for the changes of the refractive index Δn as a function of excitation density. Figure 5 is a comparison of measured and calculated spectra for room temperature GaAs under laser excitation.[8] One sees that the linear (low-intensity) absorption shows a strong increase with increasing energy above 1.4 eV, which is close to the fundamental absorption edge at room temperature. For higher light intensities, i.e., for higher excitation densities, the overall level of the absorption decreases. Since, technically speaking, absorption and refraction are the imaginary and the real parts of one and the same physical quantity (the optical response function), one can obtain the dispersive changes (inserts in Figure 5) directly from the absorptive changes. It is important to note that the dispersive changes have their extremum energetically below the fundamental absorption edge, where the semiconductor absorption is quite low. This is the main reason why it is possible to have mainly dispersive optical nonlinearities in semiconductor devices at energies where one has a relatively low absorption level. Without going into any

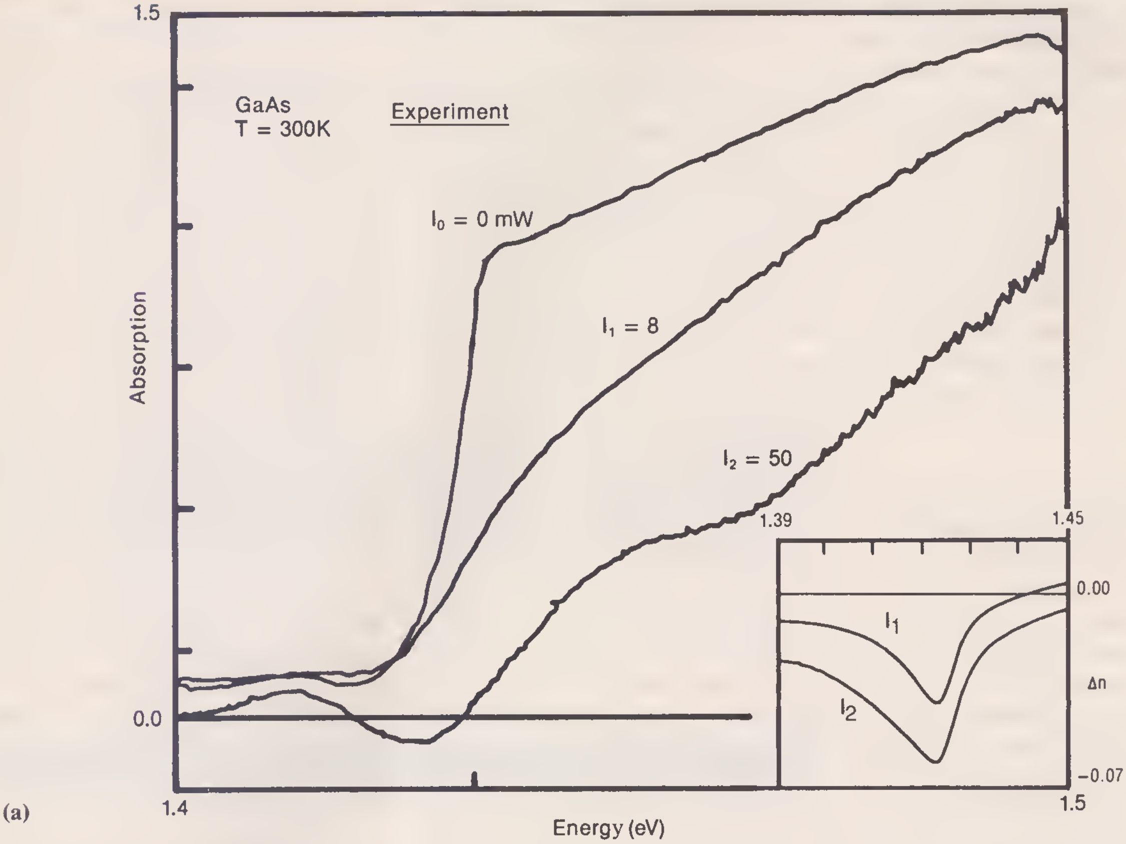


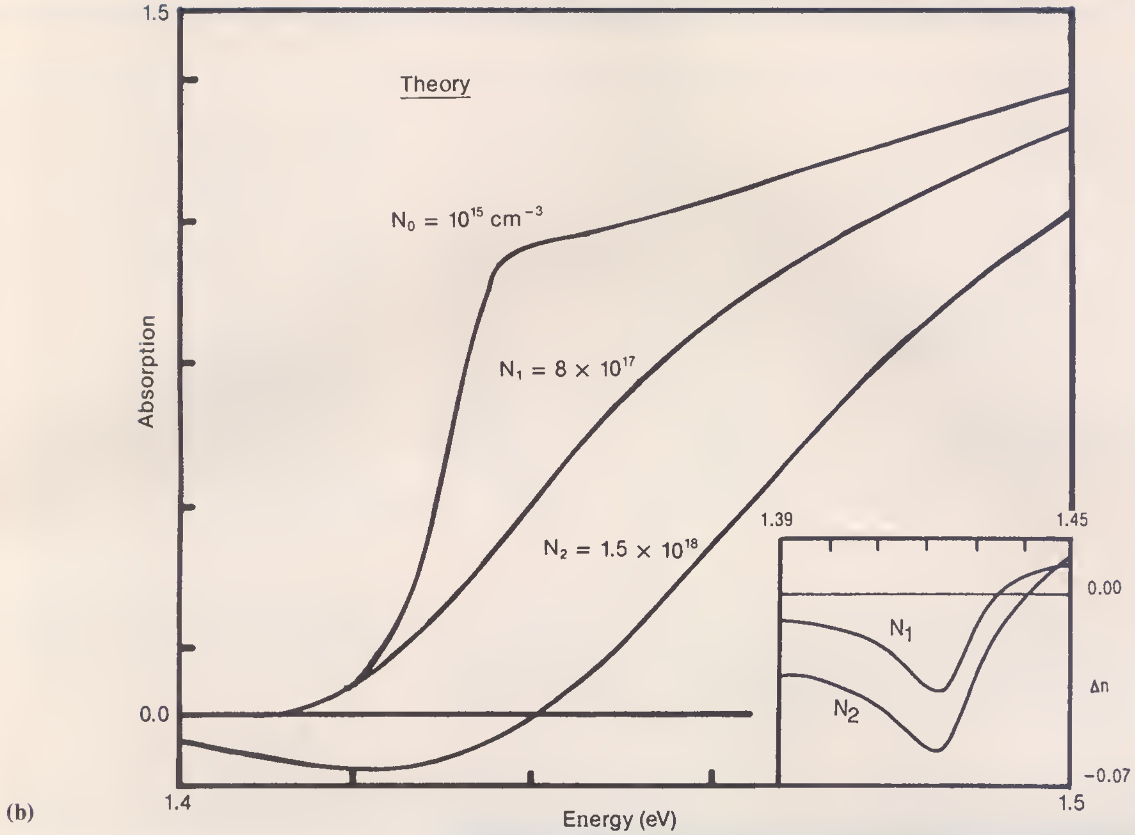
Figure 5. Comparison of experimental and theoretical absorption and refractive index spectra for room temperature GaAs. The experimental absorption plots (a) are labeled with the excitation power in milliwatts for a 15-μm-diameter spot on the sample. The excitation frequency is inside the absorption band. The theoretical absorption plots (b) are labeled with the electron-

more details, we want to emphasize that the overall agreement between theory and experiment shown in Figure 5 is quite good, and we can now use these results in further calculations and device modeling.

The importance of using the plasma theory for our model of nonlinear etalons is that it realistically includes both the dispersive and absorptive changes in the material. Even though our calculations are quite realistic where the electronic nonlinearities are concerned, they make some idealizing assumptions that might require greater sophistication at later stages: (1) We assume the optical energy is incident in the form of a broad plane wavefront and thus neglect effects of real transverse beam profiles,[2] and (2) we neglect thermal effects that are a consequence of the above-mentioned nonradiative recombination and that tend to reduce the electronic nonlinearities. Experimentally and in real applications, however, one can also largely suppress thermal effects in GaAs devices, typically by using pulsed signals of no more than a few microseconds' duration. In any case, the predictions of our model should be considered ideal performance limits as would be found in devices with effective heat sinking.

Optical bistability in semiconductors

Using the model above for semiconductor nonlinearities, it is now possible to do simulations of experimental configurations and even to explore operating regimes and device parameters that have not been tried experimentally. As the plots in Figure 5 show, the changes in the optical properties of GaAs with varying levels of excitation are rather complex. An important early goal of our work, therefore, was to optimize the performance of etalon devices in terms of a few fundamental operating parameters. Some earlier work on optimizing nonlinear etalons[9] used a purely dispersive model allowing analytical solutions. In the more realistic case, which includes dispersive and absorptive effects, it is not possible to treat the problem analytically and numerical methods must be used. To rapidly try many values of a chosen parameter, we simulated the devices in steady state. By *steady state* we mean that the incident intensity is varied so slowly that the carrier



hole-pair densities N (cm^{-3}). The inserts show the corresponding dispersive (refractive index) changes obtained by a Kramers-Kronig transformation of the absorptive changes.

density in the material is always at its equilibrium value for the chosen intensity of light in the material. The device is bistable if the plot of the output intensity versus the input intensity yields a characteristic S-shaped curve as shown in Figure 6. The negatively sloping region between the upper and lower branches of the curve is an unstable region that the system cannot normally achieve. In finite time operation, the device can only be on the upper or lower branch for those input intensity values—hence the bistability of the device.

A critical parameter in operating a semiconductor etalon is the initial resonance frequency (detuning) of the etalon. This frequency is determined by the optical thickness of the Fabry-Perot as described earlier. We modeled the GaAs etalon in steady-state operation for a large range of

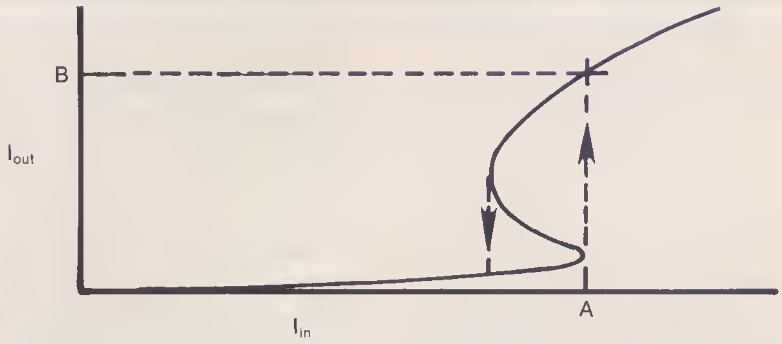


Figure 6. Input intensity versus output intensity for a steady-state simulation of an etalon. The arrows indicate switch-up and switch-down for the dynamic response. Point A is the input intensity at switch-up and point B is the output intensity after switch-up.

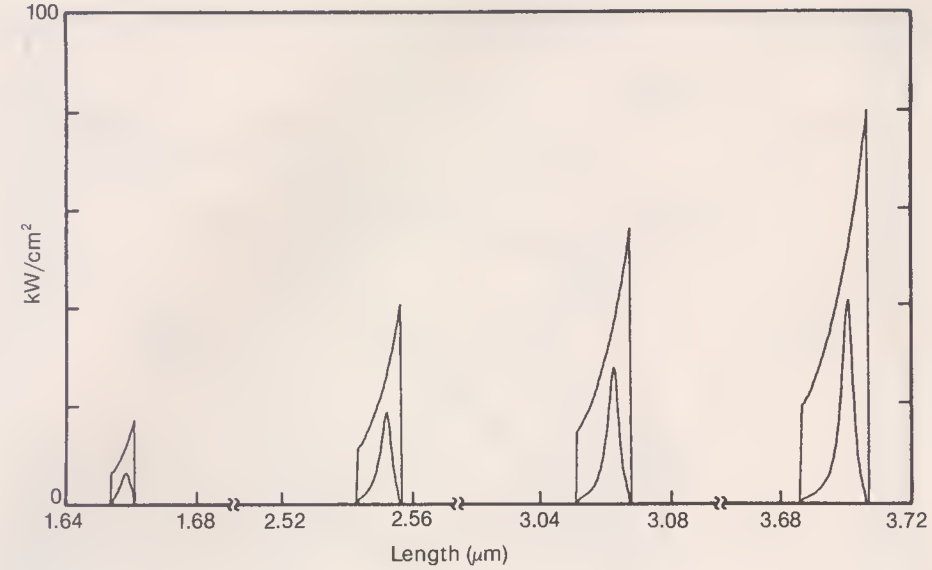


Figure 7. Calculated switch-up input intensity (upper plot) and transmitted intensity after switch-up (lower plot) as a function of GaAs etalon thickness (which determines the resonant wavelength of the etalon).

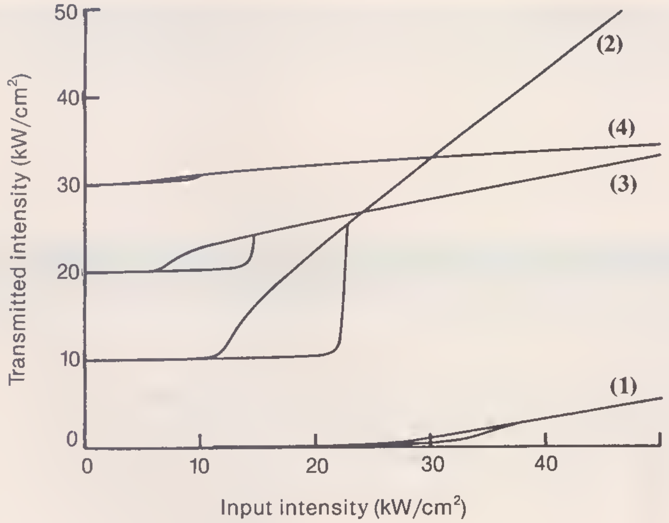


Figure 8. Transmitted intensity versus input intensity for a triangular incident pulse of 1 μs full width. The excitation energy $\hbar\omega = 1.4032$ eV; the resonator length L decreases from curve 1 to curve 4, giving rise to the respective detunings of the etalon resonance from the laser energy of -0.0170 eV (1), -0.0142 eV (2), -0.0115 eV (3), and -0.008 eV (4). The mirror reflectivity $R = 0.9$ and the carrier relaxation time $\tau = 10$ ns. The baselines for the transmitted intensity in curves 2, 3, and 4 have been shifted by 10, 20, and 30 kW/cm^2, respectively.

optical thicknesses to determine if there was an optimum initial detuning. Figure 7 illustrates the results of such a calculation. The two curves superimposed in Figure 7 are points taken from the steady-state bistability curve as illustrated in Figure 6 for each optical thickness. The upper curve in Figure 7 is the incident intensity required for switch-up measured at point A in Figure 6. The lower curve is the transmitted energy after switch-up as measured at point B in Figure 6. One can see for the series of scans in Figure 7 that there is a definite maximum transmission detuning for the etalon. Higher-transmission operation is crucial for contrast between the high and low device states in either transmissive or reflective operation. High transmission also makes it easier to obtain differential gain, which will be discussed later. The detuning for maximum transmission is unfortunately not the same as the detuning for lowest incident switching intensity. Therefore, device design tradeoffs are necessary between low switching intensities and high transmission; of course, both are important for system applications. The predicted high-transmission operation is due to a combination of the dispersive and absorptive properties of GaAs. In this case, the detuning of the etalon is initially far enough away from the excitation frequency that the intensity in the cavity has built up to the point that the absorption is saturated by the time the device has dispersively tuned through resonance.

Figure 8 shows calculated dynamic hysteresis loops for a variety of etalon detunings and incident light pulse lengths. Since the total change in carrier density in the material is related to the total energy in the light pulse, switching intensities are higher for the shorter pulses. It is also interesting that the shape of the hysteresis loops changes with the pulse width.

The reflected signal from the front face of the semiconductor etalon also exhibits a bistable response to the input light intensity. Figure 9 shows a bistable loop in reflection for the same conditions as the transmission loop (2) in Figure 8. Both the reflected and transmitted signals are present simultaneously. Figure 9 makes it apparent that the reflected signal is a negating function. For low intensities the reflectivity of the etalon is very high; if the switching threshold is passed, the device becomes highly transmitting and the reflected signal goes low. The device could function as a NOR or NAND gate, depending on the bias and signal levels used.

The switching powers predicted by the model agree well with experimental results. Typical values are less than 10 milliwatts of peak power.

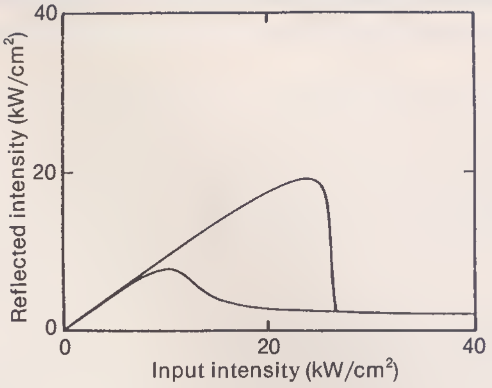


Figure 9. Reflected intensity versus input intensity for the same conditions as in Figure 8 (2).

Optical logic gates

Certain logic operations are possible with a nonlinear etalon operating as a bistable device. Since the device will maintain one of two discrete output states for some range of input intensity, it is possible to use the device in a latched mode. In that case the device would be biased by a holding beam that has an intensity positioned between the switch points on the bistable loop. The switching pulse that actually is the input logic pulse (or pulses) then only has to be sufficiently large for the total incident intensity to exceed (for a sufficient time) the switch-up threshold. The device, once switched, would remain in a high-transmission state until turned off by an interruption of its bias power or by some other mechanism. One advantage of the latched operation is the ability to hold the logic output state for a longer time to simplify the problem of synchronizing the gates with the arriving light pulses. By "clocking" the bias onto the devices, one can control and synchronize bistable devices even when their response time is much slower than the propagation time of the signals between gates.[10]

Another advantage of the latched operation is the ease of obtaining differential gain. When a nonlinear etalon is operated as a passive device, it obviously has no overall gain relative to the *total* power incident on the device. However, it is possible to achieve differential gain, in which the device is able to transmit (or reflect) a larger signal than the pulse used to switch it. Part of the output energy comes from the transmitted portion of the bias. In this case the bias energy is treated as a power supply for each device, and only the switching pulse must come from the previous devices in cascaded operation. We can illustrate the concept by referring back to Figure 4. If the bias beam intensity is at point B on the input intensity axis, then an additional pulse that brings the input intensity to point C will switch the device up to a high-transmission state. In this state the transmitted part of the bias beam can easily be larger than the intensity of the switching beam, effectively having gain when compared with the switching beam intensity. Once the switching pulse is over, the input intensity will be back at point B and the etalon will remain switched to high transmission because the input intensity has not decreased below the switch-down intensity at point A. Gain is needed to provide the optical logic gates with some amount of fan-out, so that by splitting the output beam, the device can communicate to more than one subsequent logic device. In the bistable or latched operation the ability of the device to be held in the high state after switching makes it possible to control the length of the transmitted pulse by the length of time the bias is held. This allows the restoration of the full switching pulse in time, without losing energy while the device is switching on or off and is not at the full high state.

We simulated the use of bistable devices as latched logic elements as shown in Figure 10. In Figure 10a the device modeled is operating as an OR gate with the switching pulse being superimposed onto the longer and lower-intensity bias pulse. We deliberately made the switching pulse a short, high-intensity pulse compared to a much longer bias pulse to have good time resolution in studying the switching dynamics and to more easily illustrate the differences in the roles of the bias and switching pulses. In practical applications the transmitted pulse after switch-on would need to be identical to the switching pulse with some gain. There is a limitation on how much differential gain one can obtain from a bistable device. This is illustrated in Figure 10b, which shows that as the switching pulse is decreased toward the minimum steady-state switching threshold, the response of the system slows down and the switching of the device is delayed.

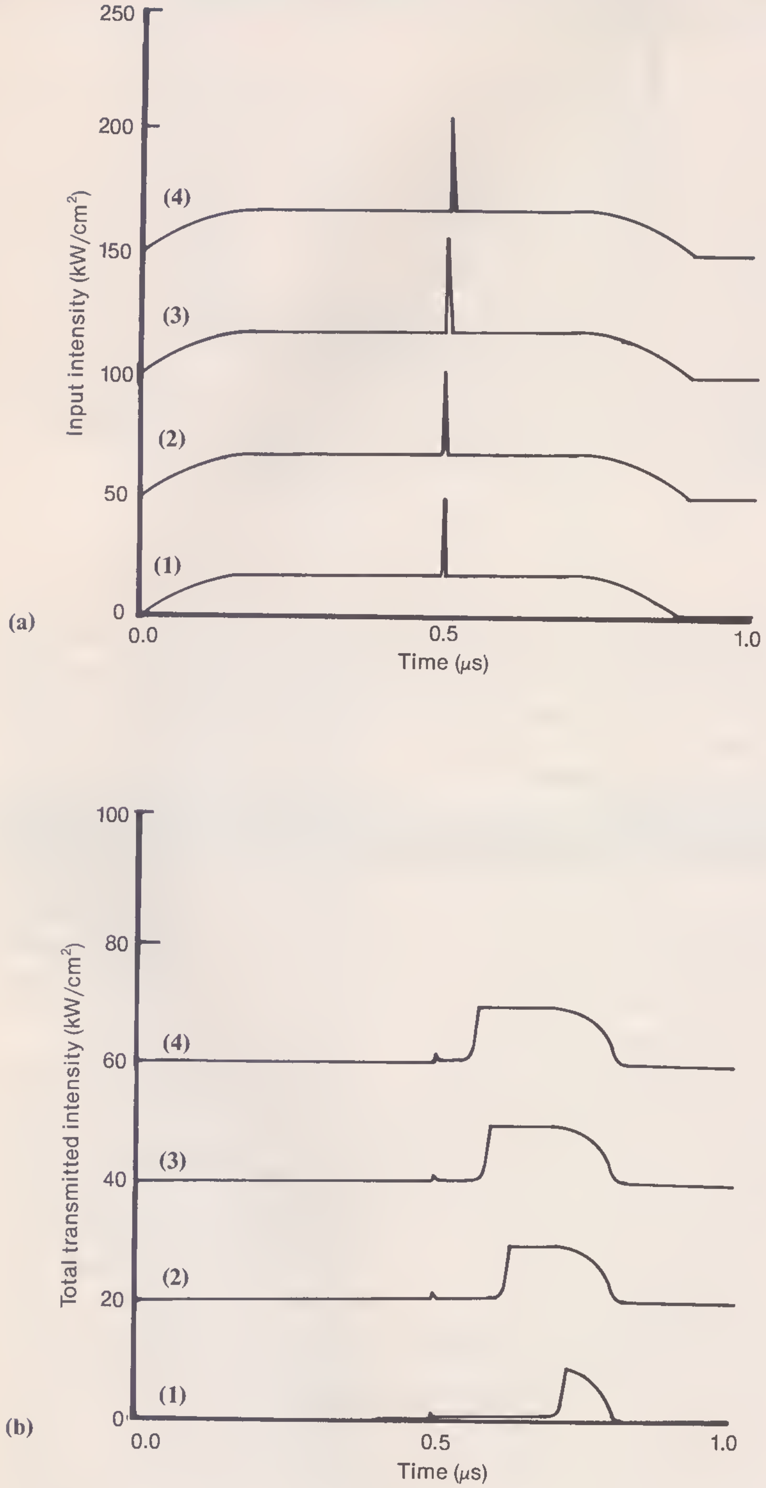


Figure 10. Latched OR gate operation modeled for a GaAs etalon. The input pulses (a) consist of a short switching pulse and a longer bias pulse. The device parameters are the same as for Figure 8 (2). The switching pulses are increasing by 2 kW/cm^2 in intensity from curve 1 to curve 4. The transmitted pulses (b) show increasing delay for the smaller switching pulses. The baselines for curves 2, 3, and 4 have been shifted by 10, 20, and 30 kW/cm^2, respectively.

This is the well-known effect of critical slowing down, which is characteristic of first-order phase transitions such as optical bistability. To get larger values of differential gain in the devices, it is necessary to set the bias closer to the switch-on point of the bistable curve and use the smallest switching pulse possible. The time response of the device is then slowed by the effect of critical slowing down. Consequently, for latched operation of bistable devices, another compromise is necessary between the two desirable features of speed and high gain.

The stability of the light signals for bistable logic devices is important to reliable device operation, especially if gain requirements lead to biasing close to the switching threshold. In Figure 11 computer simulations of the effect of a drop in the bias intensity show that a small drop is not sufficient to turn the device off. As in the switch-on process, a minimum duration of intensity change is necessary to turn off the device, making the switch-off behavior quite similar to switch-on.

Timing skew due to unequal propagation times of signals and jitter due to random variations in device response are both problems of concern in fast electronic systems. It is sometimes claimed that optical systems would be free of these problems. This is not entirely true, although timing problems should be more manageable. The linear optical elements used in an optical system can be made free of skew by provision of equal optical paths for signals through the system. For lenses this is an inherent property, but some components, such as beamsplitters, prisms, and holographic optical elements, will require careful compensation for the optical path differences these devices would produce. The nonlinear devices can be expected to have variations in their response times in a system. The effects of jitter in the input signal arrival times are illustrated in Figure 12. The single large input pulse is the superposition of two coincident pulses, which are delayed relative to each other in the other plots. Under the assumed operating conditions, the system would tolerate temporal mismatch on the order of half a pulsewidth. Larger mismatch inhibits the switching. If the design and operating parameters of a semiconductor device are specified, the system tolerances necessary for their application can be studied with computer simulations such as those in Figure 12.

It is evident from our earlier discussion that the actual complete switching time of a latched bistable logic gate must be longer than its nonlinear response time. The switch-up time of a GaAs etalon has been measured as extremely fast, on the order of one picosecond. The switch-off time of the devices is much slower. It is determined by the carrier lifetime in the semiconductor, which causes a switch-off of a few tens of nanoseconds in typical devices tested to date. It is possible to use different fabrication processes to reduce the carrier lifetime in the devices by increasing carrier recombination. Device relaxation times of less than 100 picoseconds have been demonstrated. There is, however, a major drawback to this idea for latched bistable devices. When the light pulse is longer than the carrier lifetime, reducing the carrier lifetime in the material increases the intensity necessary to create the carriers that make the device switch. Therefore, for latched operation, in which the time after switch-up and before switch-down must be long enough to restore the original switching pulse, high-speed and low-power operation must be carefully balanced with the carrier lifetime.

A possible alternative approach to etalon logic is to operate the devices in a transient regime where the devices are not latched and bistable operation is not even necessary. In this case one operates at a different detuning where the input-output characteristic is monostable, as in Figure 3, or one applies a bias to use the bistable device on the switch-up side of its hysteresis curve, which now functions as a threshold. The switch-down response of the device is still determined by the carrier lifetime, but the much shorter light pulse can be well on its way by then. The operating frequency of the individual device is again determined by its relaxation time (disregarding thermal limitations).

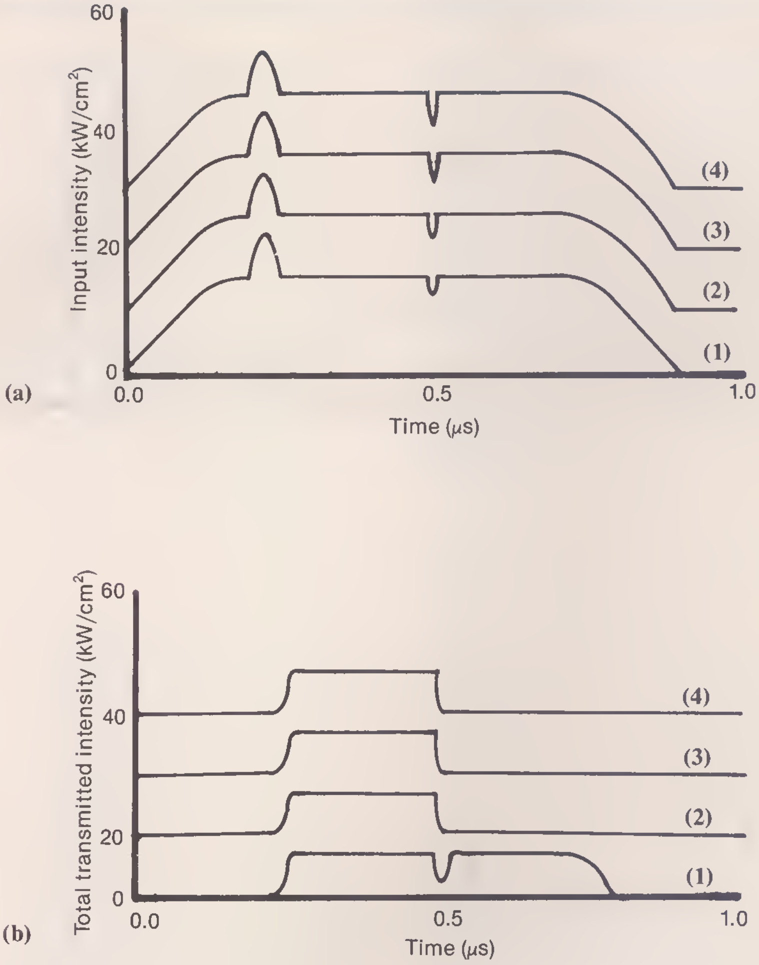
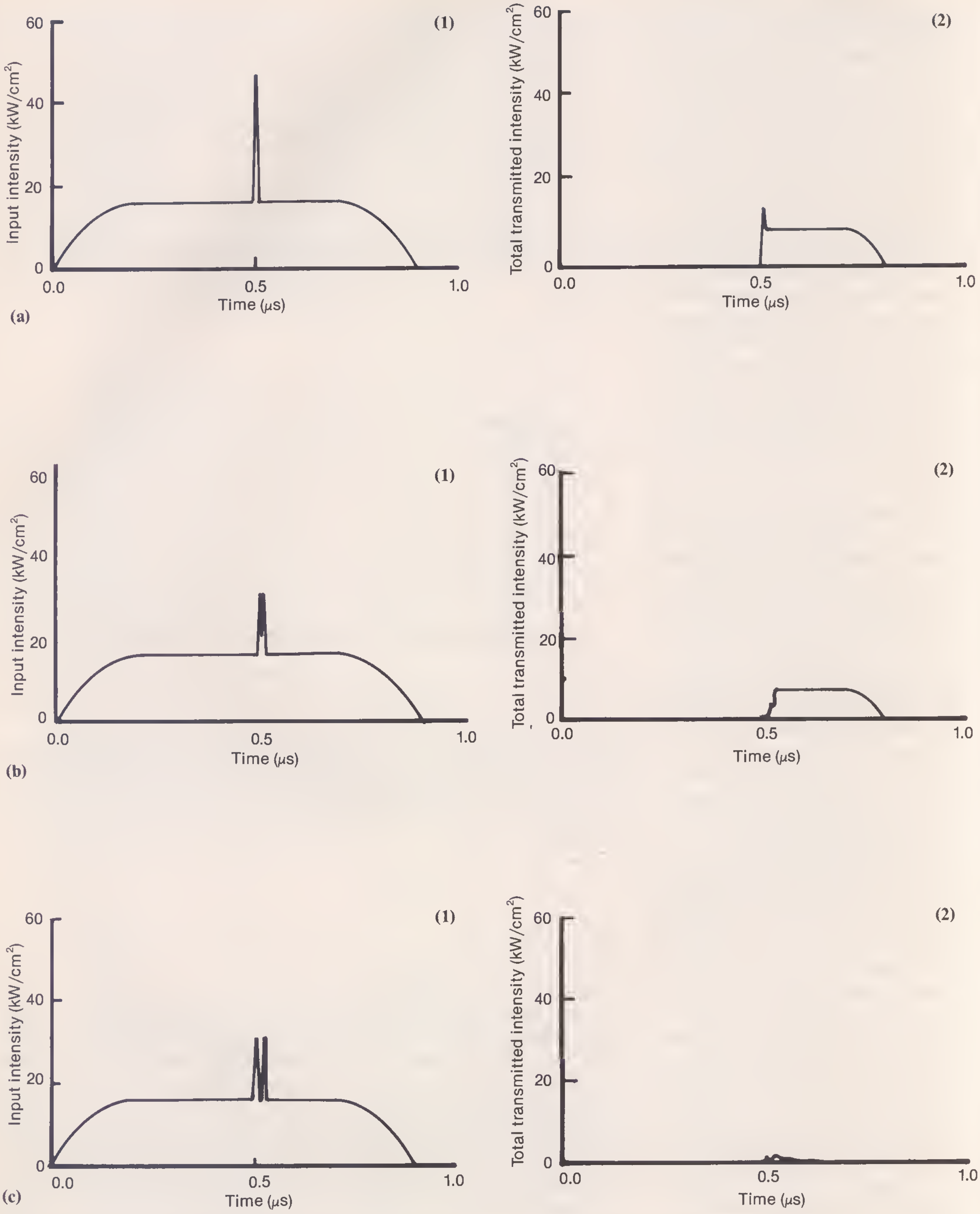


Figure 11. Simulation of effects of bias power fluctuations on latched OR gate operation. The initial short switching pulse is superimposed on a longer bias pulse with a small dip in intensity (a). The intensity dip in the bias pulse is 1 kW/cm^2 larger from curve 1 to curve 4. The transmitted pulses (b) indicate a threshold for switching off due to such fluctuations. The baselines for curves 2, 3, and 4 have been shifted.

Since the light pulses used for transient operation can be much shorter than the carrier lifetime in the material, the techniques mentioned earlier for reducing the carrier lifetime can be applied. The short pulses require high intensities to achieve the needed pulse energies, but such pulses are readily created with several types of laser systems. A major concern with transient operation is whether or not it is possible to achieve useful differential gain and restorable logic operation. In transient operation the bias pulse is used to bring the device close to the switching threshold, and the nearly coincident switching pulse must be sufficient to push the device over the threshold. To obtain differential gain, the etalon must transmit enough of the bias pulse to more than compensate for the loss in the transmitted switching pulse. To achieve restoration of the switching pulse, the bias pulse must be longer than the switching pulse so that the narrowing of the switching pulse is compensated for. These conditions make the requirements for pulse length, shape, and energy in a hypothetical system somewhat stringent.

The discussion so far has assumed that all the incident light on an optical logic device is of the same wavelength. In consequence, it is not possible to tell which part of the output signal came from the bias or from the switching beams. However, it is also possible to operate nonlinear semiconductor etalons with two different light wavelengths. The first wavelength (the pump beam) is the switching signal and is chosen such that it encounters high absorption inside the absorption band of the semiconductor, where carriers are generated very efficiently. The second wavelength (the probe beam) is chosen in


(a)
(1)
Input intensity (kW/cm²)
60
40
20
0
0.0
0.5
1.0
Time (μs)
(2)
Total transmitted intensity (kW/cm²)
60
40
20
0
0.0
0.5
1.0
Time (μs)
(b)
(1)
Input intensity (kW/cm²)
60
40
20
0
0.0
0.5
1.0
Time (μs)
(2)
Total transmitted intensity (kW/cm²)
60
40
20
0
0.0
0.5
1.0
Time (μs)
(c)
(1)
Input intensity (kW/cm²)
60
40
20
0
0.0
0.5
1.0
Time (μs)
(2)
Total transmitted intensity (kW/cm²)
60
40
20
0
0.0
0.5
1.0
Time (μs)

the highly transmitting regime of the semiconductor absorption spectrum. This light, which does not significantly affect the device, acts essentially as a probe of the state of the etalon. The principle of operation is the shifting of the Fabry-Perot resonance peaks in response to the highly absorbed pulses, thereby modifying the transmission at the wavelength of the probe pulse. The response of the device must be such that the absorption of the input pulse or pulses changes the refractive index at the probe wavelength enough to shift the wavelength of the transmission peak of the etalon by about the width of the transmission peak. For example, if the etalon is initially tuned to the probe wavelength, a NOR gate operation results if the switching pulse is able to detune the etalon from the probe wavelength.

The advantages of this two-wavelength operation are that it is very efficient in its use of switching energy and that the etalon can have different properties for the two different wavelengths of light. The two wavelengths have different absorption in the etalon, and the mirrors can have different reflectivities for the two wavelengths. For the highly absorbed wavelength the mirror reflectivity should be lower to match the absorption losses and allow efficient coupling of the switching energy into the etalon even when the Fabry-Perot peak is shifting. For the probe wavelength the absorption is very low, and high contrast in the transmitted signal is desirable. The use of higher-reflectivity mirrors can give the etalon a very high quality, and the resulting sharp Fabry-Perot peaks produce very high contrast in the output signal. A two-wavelength device can be used in either latched or transient operation. Since the probe beam does not provide the switching energy and is not highly absorbed, achieving differential gain and

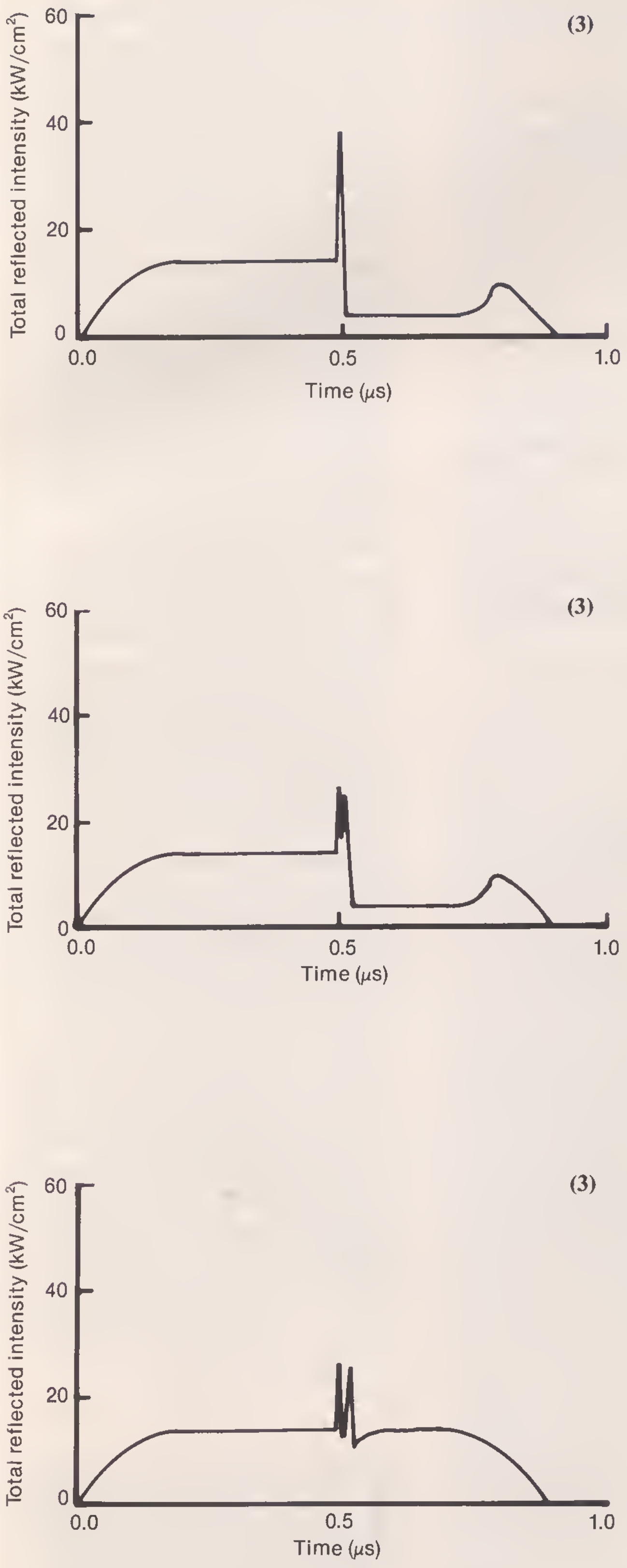


Figure 12. Modeling of pulse timing effects for AND gate operation with a GaAs etalon. Plots 1, 2, and 3 are of input pulses, transmitted intensity, and reflected intensity, respectively. In series a, the switching pulses are coincident. In series b and c, one pulse suffers a delay, increasing by 10 ns. The device parameters are again the same as in Figure 8 (2).

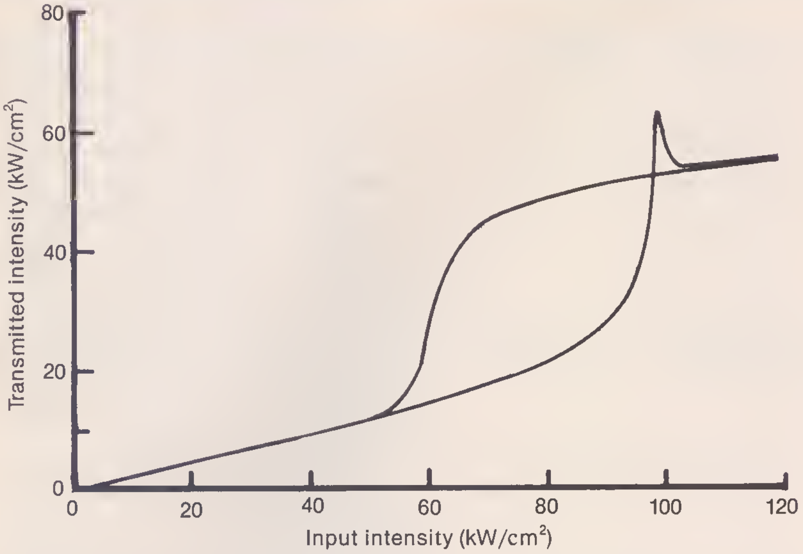


Figure 13. Output intensity versus input intensity for a 200-μm GaAs etalon. The excitation energy is at $\hbar\omega = 1.3778$. The mirror reflectivity $R = 0.3$ and carrier relaxation time $\tau = 10$ ns.

restoration of the input signal in transient operation can be much easier. Energies of less than three picojoules have been used to switch this kind of device. This is a large value compared with some electronic devices, but it compares well with the nanojoule energies needed for single-wavelength switching of GaAs etalons.

The major difficulty with the two-wavelength operation is obviously that the output signal is not the same wavelength as the input signal. This is a more serious problem than just requiring more than one light source. Since the output beam is the longer wavelength, it is not at an appropriate wavelength to switch a subsequent identical device. For any useful application of two-wavelength operation to restorable logic systems, it must be possible to use either of the two wavelengths to switch the device with similar performance. A material with a sharp, isolated absorption feature that can be readily saturated by light of slightly higher or lower energy is needed. Then the switch pulses can be on the absorption peak and the probe transmission shifted in one device with the wavelength exactly interchanged in the next. Thus, only two kinds of devices and sources are needed. If such a material can be developed, two-wavelength operation may become a practical approach in the future.

Waveguide devices

So far this discussion has concerned the physical operating principles of nonlinear etalon devices. There are actually two forms of the devices considered for application. One can easily visualize two-dimensional arrays of thin etalons that would be addressed by holographic optical elements. High-performance optical computing systems based on such arrays of nonlinear switching elements have been proposed. The major benefit of this scheme is the ability to take advantage of the natural parallelism of optics. Even moderately fast devices could use massive parallelism for enormous computational throughput. All the simulations described so far in this article have been for this kind of device, with a thickness of a few micrometers. Another form is a waveguide etalon, in which the end faces of the waveguide are mirrors just as in the etalon array, but the etalon is a waveguide hundreds of micrometers long. In this case the waveguide structure provides transverse confinement of the light, which would otherwise be lost by diffraction in an etalon of such length and small cross section. A waveguide structure is a common component of integrated optical circuits and can be fabricated by the well-developed planar microlithographic technologies used for electronic and optoelectronic devices and circuits. An optically bistable waveguide could be used as a switching or logic device for such integrated optical circuits. Planar waveguide structures would not be compatible with parallel operation on large two-dimensional arrays of optical data but would be entirely suitable for use with large amounts of serial data. After all, a major application of optics to data and signal processing today is high-speed serial transmission of signals via fiber-optic systems.

We modeled optical bistability in GaAs waveguide etalons using the same nonlinear Fabry-Perot model as for the thin etalons. This is a simplistic approach that totally ignores the mode structure of the waveguide. However, since the main effect of the waveguide is to confine the light to the waveguide boundaries, it seems a reasonable first approximation. The plot in Figure 13 shows a dynamic optical bistability calculation for a GaAs etalon 200 micrometers long with 30 percent reflectivity mirrors (the reflectivity that the cleaved ends of a waveguide would have without additional reflective coatings). Recent experiments have observed optical bistability of electronic origin in waveguides formed from GaAs and AlGaAs multiple-quantum well structures.[11] In these experiments the cleaved ends of the waveguides acted as 30 percent reflectivity mirrors. Further experiments and simulations should demonstrate device operations like those described earlier for thinner etalon devices. For waveguide-based bistable devices to be applicable, significant switching power reductions will be needed and the efficiency of coupling light into the waveguides must be higher.

Using a newly developed model, we have explained the operating principles and possible applications of nonlinear Fabry-Perot semiconductor etalons as all-optical logic devices.

We have shown some recently predicted capabilities of GaAs etalons. We have also explained some of the trade-offs necessary for the design and operation of devices with desirable qualities such as speed, gain, and low-power operation. Semiconductor etalons have potential application as all-optical logic gates for parallel-processing schemes, utilizing large two-dimensional arrays of optical switching elements, and for serial processing of data as logic devices for integrated optical circuits compatible with fiber-optic data transmission.

Each application has its own set of problems to be solved before system implementation becomes possible. Switching power or energy levels need to be reduced to make large parallel systems realizable and to make waveguide devices compatible with small signal levels. With present switching energy requirements, large arrays of etalong devices ($\cong 10^6$ elements) operating at high speed (gigahertz) would have to dissipate large amounts of heat. This is an especially difficult problem because the etalons are very sensitive to temperature changes. One approach for the large arrays is to fabricate extremely small etalons (about one micrometer in diameter) so that small energies are required to achieve the needed intensity levels.[12]

Uniformity is crucial for large arrrays of semiconductor etalons and work is continuing to improve that. For the waveguide devices, the losses of coupling light into etalons of such small lateral dimensions are a major concern. For the two types of structures the amount of differential gain that is practically realizable with high-speed operation is very important. The larger the possible fan-out, the easier it is to apply the devices to usable systems. In addition to the semiconductor etalons themselves, other components and techniques needed to create complete optical processing systems, such as light sources and spatial light modulators, must be improved or developed. The large investments already made in optical technology for serial data communications and for optical disk-based data storage make these developments more probable.☐

Acknowledgments

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Mial E. Warren is currently a PhD candidate at the Optical Sciences Center at the University of Arizona. He is interested in the design and fabrication of nonlinear optical and optoelectronic devices and materials.

Warren received his BA in physics, chemistry, and mathematics from William Jewell College in 1980, and an MS in physics from Rice University in 1983.

Stephan W. Koch is associate professor at both the Optical Sciences Center and the Physics Department of the University of Arizona. His research interests include solid-state theory, optical properties of semiconductors, many-body effects, quantum confinement effects in semiconductors, optical bistability, dynamical instabilities and chaos, coherent effects in semiconductors, semiconductor laser theory, and nonlinear devices for optical signal processing.

Koch received the PhD in 1979 and the Habilitation in theoretical physics in 1983, both from the University of Frankfurt, Federal Republic of Germany.

Hyatt M. Gibbs has been a professor of optical sciences at the University of Arizona since 1980. He is also director of the Optical Circuitry Cooperative, an NSF, industry, and university cooperative research center; and 1988 chair of the Laser Science Topical Group of the American Physical Society.

Gibbs received the 1984 Michelson Medal of the Franklin Institute for his experiments on self-induced transparency, neoclassical theory of radiation, superfluorescence, and optical bistability. He is a fellow of the APS, OSA, AAAS, and Franklin Institute, and a senior member of the IEEE.

Gibbs received the BSEE and BS in engineering physics at North Carolina State University in 1960, and the PhD in physics at the University of California, Berkeley, in 1965.

Readers may write to Warren at the Optical Sciences Center, University of Arizona, Tucson, AZ 85721.

CHI'88

Conference on
Human Factors in
Computing Systems

Omni Shoreham Hotel
Washington, D.C.
May 15-19, 1988

The annual CHI conference is the leading forum for the presentation of original designs and research in all aspects of computer-human interaction. The program this year will consist of 25 pre-conference tutorials and workshops on May 15 and 16, followed May 17-19 by technical paper and panel sessions, live and video demonstrations of user interface design, special interest group meetings, poster sessions, a doctoral consortium, and a book exhibit.

CHI '88 is especially pleased to announce that this year's invited keynote speakers include Fred Brooks, Jr., author of *The Mythical Man-Month*, and Nicholas Negroponte, director of the MIT Media Laboratory.

Washington in May is a perfect time to experience a diversity of cultural, educational, and recreational activities. The Omni Shoreham Hotel is centrally located to provide easy access to the city and its environs, and is directly adjacent to the Washington rapid transit line. Make your plans now to join us in May in the nation's capital.

The conference is sponsored by the Association for Computing Machinery's Special Interest Group on Computer and Human Interaction (ACM/SIGCHI) in cooperation with the Human Factors Society and ACM/SIGGRAPH.

CHI '88 Tutorials

SUNDAY, MAY 15

HALF DAY, AFTERNOON SESSIONS

Workshop in User Interface Design
(Tyler Blake, California State University, Northridge, CA)

Case studies, interactive class exercises, and simulations addressing practical problems and techniques in the design of user interfaces.

Rapid Prototyping for User Interface Design
(Daniel J. Rosenberg and James Wilson, Eastman Kodak, Rochester, NY, and Michael A. Nelson, Nelson Associates, Yellow Springs, OH)

Introduction to the rapid prototyping approach to designing user interfaces--advantages and disadvantages, major classes of prototyping tools, and combining prototyping with traditional life cycle methods.

Neural Networks and the Human-Machine Interface
(Charles C. Jorgensen, Thomson-csf, Palo Alto, CA)

A general introduction to neural networks plus discussion of areas in which they are applicable to human-computer interfaces, such as pattern recognition, natural language, task allocation, and robotics.

Design and Use of Hypermedia Systems
(Robert Akscyn, Knowledge Systems, Murrysville, PA)

Introduction to terminology and concepts of hypermedia (and hypertext) systems, alternative design approaches, and examination of current hypermedia systems.

The Current Psychology of Programming
(Bill Curtis, MCC, Austin, TX)

Recent research results on psychological aspects of programming, cognitive processes, experimental results, and field research with implications for software development technology and environments.

HALF DAY, EVENING SESSIONS

An Overview of Artificial Intelligence
(Elliot Soloway,Yale University, New Haven, CN)

Introductory tour of the key techniques of artificial intelligence and the types of problems for which they are appropriate.

Evaluating a User Interface
(Andrew Monk, University of York, England)

Introduction to techniques for evaluating user interfaces both before and after development.

Design and Implementation of Online Help Systems
(Greg Kearsley, Park Row Software, San Diego, CA)

Introduction for human factors specialists and software designers to the major design and implementation considerations in building an online help system.

Interfaces to Educational Software
(Wendy E. Mackay and Mark Ackerman, Massachusetts Institute of Technology, Cambridge, MA)

Examination of interface techniques being used in highly interactive, visually-oriented, college-level computer instructional systems, including examples of several systems and critiques.

Designing Graphical User Interfaces
(Bill Verplank, ID TWO Product Design Consultants, San Francisco, CA)

General approaches to graphic invention for user interfaces and specific techniques for screen design.

FULL DAY SESSIONS

Human-Computer Interaction Techniques and Technologies
(William Buxton, Xerox EUROPARC, Cambridge, England, Ronald Baecker, University of Toronto, Toronto, Canada, and Brad Myers, Carnegie Mellon University, Pittsburgh, PA)

Intermediate level examination of interactive techniques via different communication channels--visual, audio, and touch; technologies and theories as they support human-computer dialogue.

Applying Human Factors Tools and Techniques to User Interface Design (Arlene F. Aucella, AFA Design Consultants, Hamilton, MA)

Introductory level view of the tools and techniques of the human factors engineer involved in user interface design and their application to the real-world product development environment.

Using Object-Oriented User Interface Toolkits
(Kurt J. Schmucker, Productivity Products International, Sandy Hook, CN)

Intermediate level introduction to user interface toolkits, such as MacApp; how to select and use them in building interfaces.

MONDAY, MAY 16

HALF DAY, MORNING SESSIONS

User-Computer Interface Design
(James D. Foley, George Washington University, Washington, DC)

Introduction to top-down design methodology for user-computer interfaces, including requirements definition and conceptual, functional, and dialogue design, with particular emphasis on graphical interfaces.

Basic Cognitive Psychology
(John Jonides, University of Michigan, Ann Arbor, MI)

An introductory tour of the range of research topics and phenomena studied by cognitive psychologists--decision-making, reasoning, memory, and perception--for those with interest (but not necessarily a background) in cognitive psychology.

Intelligent Interfaces
(James R. Miller, MCC, Austin, TX, and Robert Neches, USC Information Sciences Institute, Marina del Rey, CA)

Application of AI techniques to human-computer interfaces to make systems easier to learn and use; comparison of intelligent assistant vs. power tool approaches.

Voice Interfaces
(Chris Schmandt, Massachusetts Institute of Technology, Cambridge, MA)

Speech production and perception, speech technologies for synthesis, recognition, and digitization, and human factors issues such as appropriateness of voice channel, interruptibility of dialogues, and syntax.

HALF DAY, AFTERNOON SESSIONS

The Effective Display of Statistical Information
(Howard Wainer, Educational Testing Service, Princeton, NJ)

Introduction to rules, new techniques, and potential mistakes in displaying quantitative data to users visually; no background in this area is necessary.

Experimental Psychology and Human-Computer Interaction (Margaret Hagen, Boston University, Boston, MA)

Introduction to the results and approaches of experimental psychology applicable to user interface design, including interface design guidelines drawn from experimental results and an efficient empirical approach to evaluation of design alternatives.

Natural Language Interfaces
(James A. Hendler, University of Maryland, College Park, MD)

Introduction to the technology behind natural language interfaces; the state of practice in the area; advantages and limitations of present-day natural language systems; and situations for which natural language interfaces are appropriate.

Constraint-Based Tools in User Interface Construction
(Robert Duisberg, Tektronix, Beaverton, OR, and Alan Borning, University of Washington, Seattle, WA)

How to use object-oriented programming with constraints to construct highly visual user interfaces, including recent research on viewing, filtering, and direct manipulation algorithm animation.

FULL DAY SESSIONS

Basic Principles and Guidelines in User Interface Design (Deborah J. Mayhew, Deborah J. Mayhew & Associates, Belmont, MA)

Introductory level survey of the known guidelines and principles for designing better interactive user interfaces, for software designers and developers with little or no human factors background.

Usability Engineering
(John Bennett, IBM Almaden Research Center, San Jose, CA, Keith Butler, Boeing Advanced Technology, Seattle, WA, and John Whiteside, Digital Equipment Corporation, Nashua, NH)

Presentation of a comprehensive, systematic method for developing more usable systems and products; includes case histories and class exercise.

User Interfaces in Window Systems: Architecture and Implementation (Jerry Farrell and Mike Schwartz, Sun Microsystems, Mountain View, CA)

Intermediate level description of the state of the art in window systems and toolkits, alternative underlying architectural mechanisms, and interface facilities available to applications running in a window system.

User Interface Management Systems
(Dan R. Olsen, Jr., Brigham Young University, Provo, UT, David J. Kasik, Boeing Computer Services, Seattle, WA, and James R. Rhyne, IBM Watson Research Center, Yorktown Heights, NY)

Intermediate level presentation of what a UIMS is and how it can affect the development of interactive application programs; basic issues in UIMS research; how a UIMS is implemented; and the basic UIMS dialogue models.

REGISTRATION

Registration may be completed in advance by mailing the registration form and fee before April 27, 1988. Reduced rates are available for registrations (with enclosed payment) postmarked on or before April 6, 1988. Registering before the April 27, 1988, deadline will speed your on-site conference registration. Members of ACM/SIGCHI, ACM/SIGGRAPH, and the Human Factors Society will receive an Advance Program, containing the registration form and hotel and transportation information in January, 1988. Others should contact:

Gail A. Chmura, Executive Administrator, CHI '88, 5214 Monroe Drive, Springfield, VA 22151, *chmura.chi@xerox.com*

FEES (in U.S. dollars)

	All	*On or before April 6, 1988*		*After April 6, 1988*	
	Students	Member	Non-Member	Member	Non-Member
Conference Only	$ 75	$ 210	$ 260	$ 285	$ 335
1 Tutorial Only	65	150	185	200	235
2 Tutorials Only	130	300	370	400	470
3 Tutorials Only	195	450	555	600	705
4 Tutorials Only	260	600	740	800	940
Conference + 1 Tutorial	140	310	385	435	510
Conference + 2 Tutorials	205	410	510	585	685
Conference + 3 Tutorials	270	510	635	735	860
Conference + 4 Tutorials	335	610	760	885	1035

Reader Service Number 4

STANDARDS

Editor: Helen M. Wood, National Bureau of Standards, B154 Technology, Gaithersburg, MD 20899; (301) 975-3240.

Board approves IEEE Computer Society standards activities

The following new Computer Society projects were approved by the IEEE Standards Board at its September 1987 meeting:

- P610.3, Glossary of Modeling and Simulation Terminology;
- P610.4, Glossary of Image Processing Terminology;
- P610.5, Glossary of Data Management Terminology;
- P610.6, Glossary of Computer Graphics Terminology;
- P610.7, Glossary of Computer Networking Terminology;
- P610.8, Glossary of Artificial Intelligence Terminology;
- P610.9, Glossary of Computer Security and Privacy Terminology;
- P802.9, Integrated Voice and Data (IVD) LAN Interface Standard at the MAC and Physical Layer; and
- P1162, Guide for Software Project Management Plans.

The IEEE Standards Board has approved the standards proposed by Project 1042, Guide to Software Configuration Management. This project is now completed.

The American National Standards Institute (ANSI) recently adopted the following as American National Standards:

- IEEE 854, Radix-Independent Standard for Floating Point Arithmetic, and
- IEEE 990, Ada as a PDL.

For more information on new and ongoing projects or for assistance in purchasing copies of approved standards, contact Mrs. Louise Germani, IEEE Computer Standards Secretariat, IEEE Standards Office, 345 East 47th Street, New York, NY 10017; (212) 705-7091.

Prototype data dictionary software evaluated

More than 40 users from private industry and government, both in the United States and abroad, have agreed to use and evaluate prototype software developed by the National Bureau of Standards (NBS) Institute for Computer Sciences and Technology. The software implements a draft industry standard for the Information Resource Dictionary System (IRDS). The prototype software is intended to help those involved in review, development, and implementation of the proposed standard, which is over a thousand pages in length.

IRDS is a key computer software tool that can be used to record, store, and process information about an organization's data and data processing resources. NBS has been working with other user and vendor organizations on the refinement and enhancement of the IRDS technical specifications, which are proposed for adoption as American, international, and US government standards.

Revision proposed to Fortran 77

Accredited Standards Committee X3 on Information Processing Systems is holding a four-month public review and comment period on draft proposed revised American National Standard, X3.9-198X, Programming Language Fortran.

Five major additions to Fortran 77 stand out in this proposed standard: (1) array operations, (2) improved facilities for numerical computation, (3) user-defined data types, (4) facilities for modular data and procedure definitions, and (5) the concept of language evolution. A number of other additions are also included, such as improved source form facilities, more control constructs, recursion, and dynamically allocatable arrays. No Fortran 77 features have been proposed for deletion.

The draft proposed revised standard is available for review and comment through February 23, 1988. Copies may be purchased from Global Engineering Document, Inc. by calling (800) 854-7179.

Formation of a working group on simulation

A standards working group on simulation is being organized under the sponsorship of the Technical Committee on Simulation. The intended function of the group is to define functional requirements for the construction of a reliable discrete event simulation language.

Complex simulation involves multitudes of modules that can potentially interact. The output of such a model may be meaningless and unverifiable if the functional structure of the underlying language is not configured with a set of well-defined constituents. A definition of functionality will increase the usefulness and reliability of the results of complex simulation.

The working group intends to tackle these issues. A preliminary meeting will be held in conjunction with the annual meeting of the Technical Committee on Simulation at the Winter Simulation Conference in Atlanta, Georgia, on December 15. The time and place of the meeting will be posted at the conference.

Interested parties should contact Oryal Tanir at (514) 468-5523 or circle 187 on the Reader Service Card for additional information.

Computer Society NEWS

Editor: Sallie Sheppard, Dept. of Computer Science, Texas A&M University, College Station, TX 77843; (409) 845-5466

Board approves $15.67 million budget, new transactions, Asian office

Meeting at the Loew's Anatole Hotel in Dallas on October 30, the Computer Society's Board of Governors adopted a 1988 operating expense budget of $15.670 million, up 4.5 percent from last year's budget of $14.994 million. The budget as adopted is based on income of $15.532 million, with a budgeted deficit of $138,000.

Current projections indicate a surplus in excess of $300,000 for 1987. Moreover, in each of the last three years the society has ended the year with working capital reserves exceeding the amount required by policy (5 percent of a year's expenses). In this context the board approved two major new initiatives—a new transactions and an Asian Office. Commenting on the 1988 budget, incoming President Edward A. Parrish of Vanderbilt University noted that, on the basis of past experience, the society could anticipate cost savings that would eliminate the budgeted deficit.

Transactions. As developed by Bruce Berra of Syracuse University, C.V. Ramamoorthy of UC Berkeley, and Benjamin Wah of the University of Illinois at Urbana-Champaign, the proposal for the new transactions envisions a scholarly journal, published quarterly commencing in 1989, that will report results on the research, design, and development of data engineering methodologies, strategies, and systems. Its scope includes all computer science and engineering areas related to the management of data and knowledge. The proposal has been supported throughout its development by the Technical Committee on Data Engineering.

The new transactions will be interdisciplinary, covering such fields as computer science, artificial intelligence, electrical engineering, computer engineering, and cognitive science. It will be aimed at users, researchers, developers, managers, government officials, and strategic planners.

Publications Vice President Tom Cain of the University of Pittsburgh is forming a search committee to identify candidates for the position of editor-in-chief.

Asian office. Following a resolution passed by the board in May, an ad hoc committee chaired by Board Member Akihiko Yamada of NEC has been studying the feasibility of establishing a Computer Society office in Asia. As reflected in its report, the committee concluded that such an office—modeled after the society's successful venture in Brussels—would indeed be feasible and further recommended that it be located in Tokyo.

Three potential locations—Tokyo, Hong Kong, and Singapore—were evaluated against criteria developed by the committee. Hong Kong was rated second, Singapore third. The target date for establishment of the office is on or before June 30, 1988.

In addition to Yamada, the committee consisted of Motoei Azuma, Waseda University, Tokyo; V.N. Balasubramanian, City Polytechnic of Hong Kong; Chung Wu Cho, Korea Advanced Institute of Science, Seoul; T.M. Elliot, Computer Society; Tadao Ichikawa, Hiroshima University, Hiroshima; S.S.S.P. Rao, Indian Institute of Technology; Roy L. Russo, IBM (Computer Society president); Lim Swee Say, National Computer Board, Singapore; Yoshihiro Tohma, Tokyo Institute of Technology; Mario Tokoro, Keio University, Kanagawa; and Chwan-Chia Wu, National Taiwan Institute of Technology, Taipei.

Division VIII nominees. As recommended by the Nominations Committee, the two nominees for IEEE Division VIII delegate-director are Roy L. Russo, outgoing 1987 Computer Society president, and Ned Kornfield of Widener University. This slate was approved by Board of Governors ballot and will appear on the 1988 IEEE ballot for the 1989-90 term.

Board vacancy. The election of Joseph E. Urban to the post of second vice president for 1988 (as reported in the November *Computer*, p. 101) created a vacancy on the 1988 Board of Governors, since Urban would be serving the second year of his two-year term on the board next year. The vacancy was filled by a board ballot, in which Paul Borrill was elected to complete the remainder of Urban's term.

Other decisions. All six proposed Computer Society Bylaws amendments (as described on p. 100 of the August *Computer*) were approved for the second time by the board. They will now be submitted to the IEEE for final approval.

Raymon Oberly, long active in the Membership and Information Board as well as in numerous other committees, was elected to fill the post of 1988 society ombudsman, succeeding Susan Rosenbaum, who has held the position for the past two years.

Duncan Lawrie of the University of Illinois was elected by the board to serve as secretary for 1988. Lawrie has served in this post throughout 1987.

Oscar N. Garcia of George Washington University, former society president (1983-84), was approved as the 1988 recipient of the Richard E. Merwin Award.

Erwin Tomash, retired chairman of the board of Dataproducts, was approved as the 1988 recipient of the Computer Entrepeneur Award.

Sumit Dasgupta of IBM was approved as editor-in-chief of *IEEE Design & Test*, succeeding Vishwani Agrawal of AT&T, who has held the post for the past two years. Dasgupta will start his term with the February 1988 issue of *D&T*.

David Pessel of Sohio was reappointed to serve a second term as editor-in-chief of *IEEE Expert*.

Late election results

With ballot count completed just at press time, IEEE Corporate Services Director Betty Stillman announced that Harriett Rigas of Michigan State University has won the election for IEEE Division V delegate-director. Her term of office is 1988-89.

Committee on Public Policy forms subcommittee on software safety

Ralph J. Preiss, COPP Vice-Chair

Appearing in the October 1986 issue of *Computer,* an article described the scope of the various subcommittees of the Committee on Public Policy. Several questions were prompted, such as "Why these subcommittees and not others?" "Under what subcommittee would you consider licensing of computer professionals?" "How about medical applications of computers, for example, in instrumentation?" "The Strategic Defense Initiative?" "Trade issues?"

Frankly, we are not prepared to cover all issues that are in the public eye relative to computers or computing. The committee is made up of volunteer members interested in sharing with their fellow members their concerns on certain computer profession-related public issues. In the process, certain positions lend themselves to becoming Computer Society positions if enough members feel the same concern, and if they agree with the position statement produced.

Some issues may be of concern one year and wane in another. For example, there was a lot of activity on immigration and engineers last year before enactment of the US immigration bill. This year, the Human Resources/Immigration Subcommittee became inactive. Other issues linger on. One case in point is the US information transfer policy, which continues to be defined, debated, and modified. Doubts are growing in the public mind over the adequacy of automation, instrumentation, and testing regarding such issues as the quality assurance, licensing, and safety aspects of computers and programs for the medical profession, navigational equipment, the space shuttle, atomic reactors, and air traffic control equipment. These doubts could severely impact the profession unless professionals stand up and speak out, in a professional way.

COPP takes action. COPP has established the Software Safety Subcommittee, chaired by Raymond P. Jefferis of Widener University, so that these topics can be taken up.

A member recently asked whether the Computer Society had initiated a study or adopted a position on the Strategic Defense Initiative similar to the position of the American Physical Society. Since it doesn't have a subcommittee on military computing or programming reliability/safety/integrity, COPP hasn't concentrated on the SDI issue. However, COPP members subscribe to a monthly IEEE US Activities Board newsletter, *Legislative Report*, which devoted a page to the APS report in its July issue. In part, this is what the APS report stated:

> "The Defense Department's timetable for deployment of early stages of the SDI was recently labeled as overly optimistic by a panel of the American Physical Society. APS did not 'debate' or challenge the Pentagon, but the release date (April 30) coincided with a report to Congress from the SDI Office outlining prospects of using particle beam weapons against incoming Soviet missiles.
>
> "The 424-page report of the American Physical Society, a 21-month study effort, was characterized as outdated by the SDI Office. The office, however, welcomed it as 'an objective, independent appraisal of various technologies,' but noted that recent advances in free electron lasers and neutral particle beams have brought these technologies closer to the required performance level.
>
> "The APS group focused its study on the science and technology of directed energy weapons. It did not address the policy of whether or not SDI should be deployed or any question of cost-effectiveness. In sum, the study group found that another decade of intensive research in laser and other directed energy weapons (DEWs) is needed before an informed decision can be

TAB focuses on self-assessment, 1988 planning

Sallie Sheppard

Self-assessment and prioritized planning for 1988 were the focus of the Computer Society's Technical Activities Board meetings, held during the late-October Fall Joint Computer Conference in Dallas.

The Study Committee chair, Ned Kornfield, reported on the results of a year-long self-assessment analysis aimed at identifying strengths and weaknesses of the TAB. For the study, the panel drew data from several sources, including a survey questionnaire mailed to four CS membership groups, a financial assessment of technical committee conferences and workshops, and a TC vitality evaluation.

The analysis of the available data identified many positive features about the society's technical activities, including the various functions of the 33 TCs. Among the activities are planning workshops and technical meetings; publishing newsletters; sponsoring special publications, such as theme issues of journals and magazines, tutorials, and bibliographies; and defining and participating in the development of standards.

Under the current organization, the TCs each address specific technical domains. The TAB is composed of the 33 chairs of the TCs, operation committee members, and representatives from the Standards Activities and other boards. The TAB is chaired by the vice president of technical activities, who for 1987 has been Ken Anderson.

Although there are many positive features of the TCs as leaders of technical activities within the society, data collected during the self-assessment study suggests that the TCs are relatively unknown among CS members and that the organizational structure of the TAB has been ineffective in supporting the TCs in carrying out their activities. A restructuring of the TAB was strongly recommended to overcome the negative limitations identified in the study.

Based on the report, Anderson led discussions of how such a restructuring might be approached in 1988. Four areas of concern were identified for further study before the next TAB meeting is held at San Francisco in February; the areas are finance, product development, planning and organization, and new initiatives.

Reorganizational ideas discussed included a grouping of TCs by functional technical area into approximately seven larger units. It was felt that such an arrangement would encourage interdisciplinary efforts between the TCs.

TAB has been exploring ways to provide improved service to attendees of workshops and conferences. Cochaired by Paul Hazan and Jon Butler, the Satellite Symposium Task Force is exploring the feasibility of a satellite symposium with attendees going to local sites linked to other sites by satellite. This would enable geographically dispersed groups to participate in joint technical activities and could provide society members with a highly cost-effective method of technical interaction.

made as to their potential effectiveness for missile defense. APS acknowledged that 'predicting the course of technological progress can be particularly difficult' but said that ...'there are significant gaps in the scientific and engineering understanding of many issues...' and 'successful resolution of these issues is critical for the extrapolation to performance levels that would be required in an effective ballistic missile defense system.' The group concluded that DEW technology faces so many uncertainties that 'deployment of a substantial DEW component in a ballistic missile system cannot be foreseen before the year 2000.' The APS report did not examine kinetic energy weapons," which are currently under consideration for early deployment.

Specific issues studied. COPP tries to avoid moving targets, such as the one described, so that a report 21 months in the making is not outdated when it finally is released. However, the committee has addressed such specific issues as the National Science Foundation budget, Section 1706 of the 1986 US Tax Law, and the copyrighting of computer screens. It has analyzed these issues, has rapidly produced position statements (in one to six months), and has made them public. Nonetheless, COPP has never attempted anything as complex as analyzing software reliability for use in SDI. But perhaps it should!

The subject was discussed at the October 30 meeting of the Board of Governors in Dallas. The sense of the discussion was that the SDI software issue is more political than technical.

Since COPP is made up of volunteers who serve in their spare time, the committee is not in a position to study such a long-term issue. Considerable resources would have to be spent to formulate a position, and such resources are beyond the means of the society. Still, COPP could comment on the SDI position statements of other organizations, if a distortion of technical findings is involved.

COPP seeks and welcomes your professional opinions on this subject. Those who would like to express their views are invited to write to Paul Davis, COPP Secretary, 41 W. Huron St., Jackson, OH 45640.

In addition, society members who would like more information on COPP or would like to participate in COPP activities are invited to circle No. 188 on the Reader Service Inquiries Card in this edition and mail it to the address indicated.

US colleges offer computer optics programs

Chuck Governale, Computer *Staff*

The University of Rochester and the University of Colorado at Boulder have established curriculums in integrated optical computing, the theme of this month's *Computer* articles. A second New York campus, the Rochester Institute of Technology, is expanding its program and is building a new Center for Imaging Science.

The computer optics curriculum at the University of Rochester is offered through its Institute of Optics. According to university officials, the institute has an international teaching and research reputation.

The institute is devoted to optics and optical engineering, and offers programs leading to the BS, the MS and the PhD degrees. Instruction and research are available in virtually every phase of optics, including optical instrumentation and design, quantum optics, laser engineering, signal processing, guided wave optics, nonlinear optics, and optical materials.

The program at the University of Colorado at Boulder is offered at the Center for Optoelectronic Computing Systems, which was formed by 20 investigators from both the University of Colorado and Colorado State University to promote research in areas where optics has a clear advantage over electronics in computing. The disciplines include chemistry, computer engineering, physics, optical systems design, and electrical engineering, among others.

Last April, the National Science Foundation designated COCS as a NSF Engineering Research Center and granted a five-year award of $14.6 million.

COCS is now building three proof-of-discipline machines to address the three major strengths of optoelectronic computing: speed, parallelism, and high connectivity.

Graduate and undergraduate students alike may participate in the center's educational and research components. The instructional program is designed to provide a systems-oriented education, involve students in research, codify new knowledge generated at the center, and develop methods for transferring knowledge to industrial and other users.

According to officials at the Rochester Institute of Technology, RIT is the only US university that offers undergraduate and graduate degrees in imaging science, a technology that is the focus of the Center for Imaging Science that is under construction and is scheduled for completion in 1989.

Groundbreaking for the $8.5-million center took place November 4. The four-story building will house classrooms, research facilities, several labs, a lecture hall, and offices.

When completed, the CIS will reportedly provide the most comprehensive academic center in North America for the study of imaging science. Work conducted there will lead to graduate as well as postgraduate degrees.

RIT has achieved national prominence in a range of programs that are the elements of imaging science, including photographic science, computer science, and engineering.

A student at work at the Optoelectronic Computing Systems Center at the University of Colorado at Boulder.

Corning experimental fiber fatigue-resistant

Altering the surface composition of the glass substantially improves an optical fiber's long-term mechanical reliability, according to Suresh T. Gulati of Corning Glass Works' Research and Development Division. He spoke at the International Society for Optical Engineering's Symposium on Fiber Optics and Integrated Optoelectronics, held August 17, 1987 in San Diego, California.

The developmental fiber Gulati described differs from standard optical fiber in that the composition of its surface layer includes an oxide dopant. Standard fiber has a pure silica surface. The dopant of the experimental fiber increases its fatigue resistance and reduces its strength variability.

Gulati's paper was coauthored by J.D. Helfinstine and G.S. Glaesmann of Corning Glass Works, and D.R. Roberts, E. Cuellar, and L.M. Middleman of Raychem Corporation.

Software offers second opinion on heart disease

Nuclear imaging procedures used to analyze coronary blood flow problems generate so much data that computers can handle the analysis more easily than can humans. Using records of diagnoses made on 291 patients, Norberto Ezquerra of the Georgia Institute of Technology Bioengineering Center and Ernie Garcia of Emory University are developing an expert system to put the knowledge and experience of human diagnosticians to work for other doctors.

When used for 50 test patients, the system agreed with human experts 90 percent of the time. Ezquerra believes that the system can both provide a second opinion and serve as a learning tool for other physicians.

Ezquerra received a five-year grant from the National Library of Medicine of the National Institutes of Health to continue development of the system. Coinvestigators include John Peifer and Mike West of Georgia Tech and Ernie Garcia, Larry Klein, Spencer King, and Gary Roubin of Emory University.

The computer animation technique relies on a 3D geometric database editor called MAX, developed at Georgia Tech. It also uses a Pixar computer, originally developed by George Lucas for special effects in the "Star Wars" movies.

Computer technology will also help the Alcohol Research Unit of the Boston University School of Public Health. A computerized questionnaire, developed by the Oakland Group of Cambridge, Massachusetts, will reportedly help the unit study the probabilities of drunken driving among the public and convicted driving-under-the-influence offenders.

The study will estimate the probabilities of driving and crashing with various levels of alcohol, identify characteristics of high-risk drinking drivers, and examine the effectiveness of treatment programs for repeat DUI offenders. The study is funded by National Institute on Alcohol Abuse and Alcoholism grants.

Parnas receives award for social responsibility

David Parnas, professor of computer science at Queen's University in Kingston, Ontario, has been awarded the first Norbert Wiener Award for Professional and Social Responsibility by the board of directors of Computer Professionals for Social Responsibility.

Parnas has been a prominent opponent of the Strategic Defense Initiative of the US Department of Defense. In 1985, he resigned from an official panel of computer experts convened by the Department of Defense to assess the SDI program. Since his resignation, Parnas has worked to educate the public and the computer profession about the limitations of computers and software, and the special dangers of the SDI proposal. (For a letter by Parnas on this subject, see Letters to the Editor in the February 1987 issue of *Computer*.)

The Norbert Wiener Award for Professional and Social Responsibility is named after Norbert Wiener, the MIT mathematician and cyberneticist. Wiener was an outspoken advocate for the responsible use of computers.

NSF initiates two research centers

The National Science Foundation has made grants totaling $2.4 million to establish two centers where engineers and scientists will develop a science base for cost-saving manufacturing processes and for software to aid in the design of better mechanical systems for spacecraft, robots, and vehicles.

With a five-year NSF grant of $400,000 annually, the University of California at Los Angeles and the University of Southern California will jointly establish a Center for Manufacturing and Automation. This grant will also fund supporting research at four associated institutions: Arizona State University, Caltech, and the Universities of California at Santa Barbara and Irvine.

The University of Iowa will receive $375,000 from NSF over five years to establish a Center for Simulation and Design Optimization of Mechanical Systems.

Researchers at the UCLA/USC center will design software for manufacturing processes and scheduling, the control of robots, the computer simulation of automated factories, and the development of "expert" systems for the design of assembly line machines. Researchers at the University of Iowa center will develop software to simulate the physical conditions in which equipment is expected to perform.

NACD plans to close hot computer market

The National Association of Computer Dealers plans to stop the flow of stolen microcomputers by joining forces with manufacturers, insurance agencies, and local law enforcement agencies. NACD is accumulating a database of serial numbers for stolen computers. The list will be available to any company or individual wanting to buy a computer. NACD plans to have the system ready by early 1988.

A computerized response system will serve members, while a voice response system will serve the public. The toll-free number for the public will be (800) 346-NACD.

Owners of stolen microcomputers can call NACD directly at (800) 223-5264 (in Texas, 713-496-3283) to report their computers' serial numbers for inclusion in the database.

NEW PRODUCT REVIEWS

Editor: Richard Eckhouse, MOCO, Inc., PO Box A, 91 Surfside Rd., Scituate, MA 02055; Compmail+, r.eckhouse

Wanted: reviewers

Departing from the theme format we've used in the last few columns, this month we look at a number of important new products and releases. I've been fortunate to pick up some new contributors who have interests in both hardware and software. Still, it's important to remind you that I need additional reviewers who can help us cover other equally important areas, such as multivalued logic, new architectures, solid-state developments, artificial intelligence, and neural networks, to name a few. We need volunteers. Please direct calls and letters to me at the address and telephone number given above.

Richard Eckhouse

Project management with Time Line

William Gleason, Martin Marietta

Project management is the organized planning and tracking of projects. To be successful, a project manager or group lead engineer must allocate resources, track costs and manpower, and manage the project critical path. These tasks must be completed as planned to keep the entire project on schedule. In simpler terms, project management is the coordination of many tasks involving people and money. Done correctly, it brings the right people together at the right places and at the right times to assure completion of the project within budget constraints. Project management software can help get the management job done more efficiently and provide the information needed to make informed decisions on project matters.

Project management software packages exhibit a wide range of features and capabilities, and a correspondingly broad price range (from $100 to $10,000). A moderately priced system can be expected to provide all of the fundamental project management tasks without all of the flourishes. The software should be easy to learn and use, have a minimum number of menu screens to contend with, allow resource and cost information to be coupled with project tasks (thereby providing resource loading capability), and have a sufficient number of reports to adequately indicate the status of the project.

Time Line from Breakthrough Software is such a product. It is the result of several years of design and development by Andrew Layman, a San Francisco project manager and programmer.

The system is accessed through a series of menus. The menus present commands which either perform a function or provide instruction. Other menu choices access forms. These forms consist of multiple choice options and simple fill-in-the-blank fields. The full system, the one reviewed here, includes both Time Line and Time Line Graphics.

Setup

Time Line can be used either on a dual floppy system or a system with a hard disk. The setup instructions in the manual are clear and the on-screen messages easy to follow.

When you initialize Time Line, you are confronted with a comfortable Lotus-style menu with commands across the top. You can select commands either by using the first letter of each selection or by using the left arrow or right arrow to move across to the desired selection.

To set up the monitor, printer, and plotter you press "S" at the main menu and follow the prompts provided by the program. Two helpful features are Sideways, a program that allows wide reports to be rotated 90 degrees before printing, and the capability to customize reports to work with several popular word processors. On-screen messages are explained in the manual.

The manual is well organized, with attractive tabs to clearly mark the sections. As with most manuals, more detail would be better, particularly when there is something you don't understand. The sidebars are plentiful and helpful. Overall, the manual provides sufficient help, in plain English.

The on-screen tutorial consists of seven lessons plus a Fast Track lesson for those familiar with automated project management. The lessons include getting acquainted, building the project environment, entering tasks, assigning costs and resources, managing resources, signing off, and managing the schedule progress.

The Schedule form is the first menu presented. When completed, it contains information about the project. You are next led to the Calendar, which allows selection of the work effort (hours,

Project management terms

Activity (task, work item)—the actual performance of a discrete task. Activities are defined in terms of resources required over a specified period of time. Each activity reflects a quantity of effort essential to the accomplishment of the project.

Event (milestone)—a point in time usually measuring the beginning or end of an activity. As such, an event cannot consume time or resources and is used only for performance measurement.

Constraint—a condition or limitation that defines the relationship between one activity or event and another.

Lag—a value that establishes the delay in a constraint relationship.

Network (functional flow diagram)—a graphic depiction of the activities and events on a project, with technical interfaces depicted. When the activities, events, and constraints have been defined, the network is analyzed by performing a forward pass using the starts of all activities and events, then a backward pass starting at the finish of each activity and event.

Float—the difference between the start and finish dates obtained from the forward and backward pass. Early dates (forward pass) are subtracted from the late dates (backward pass).

CPM (critical path method)—a term commonly applied to network-based systems using activity-oriented networking techniques and only one activity time estimate in calculating network dates and slack.

PERT—a unique technique for planning and program control that uses a pictorial representation of all the actions that must be taken and an analytical procedure for predicting performance and evaluating uncertainty for a project using a minimum, most likely, and maximum time estimate technique (called *three-time estimate*) for activity duration.

Gantt chart—a graphic representation that shows each task of a project as a bar whose length is proportional to its duration, imposed on a time-related scale. Generally, critical path, float, and progress are shown using symbology to differentiate them from planned activity.

Histogram—a graphic representation of a frequency distribution in which the widths of contiguous vertical bars are proportional to the class widths of the variables and the height of the bars are proportional to the class frequencies. It is used to show cost and resource distribution over time.

Resource—any person, equipment, or material needed to accomplish any project task.

Resource leveling—the process of adjusting resources when conflicts in availability arise.

Work breakdown structure (WBS)—a structured method of displaying all products and services that compose a program to provide the identification of work tasks. The structure generally shows hierarchical levels of detail and allows for summarization of program data.

days, weeks, months). A menu appears for each month, permitting entry of specific nonworking days (such as holidays). You can call up succeeding months by pressing the Tab key. Each menu is clear as to its purpose and the form of the data to be entered.

The next form, Resources and Costs, follows the Calendar screens. You can define resources as people, teams of people, or equipment, and schedule them all as full- or part-time. The software develops resource histograms, defining when and how fully each is scheduled. Time Line monitors the allocation of all resources and alerts you when they have been overscheduled. The resource histogram is an excellent tool for visually presenting the scheduling and overscheduling of a resource. When entering the resource data, a handy pull-down list appears if you press the F2 function key. The software *resource levels* the schedule automatically if you want to see where available resources will fit into the schedule. Another alternative is to call up the histogram, toggled by pressing the F6 key.

The Options Form screen gives you several options on how to have your schedule computed. You can choose whether or not to have the schedule recalculated automatically every time you make a change, whether to take resource availability into consideration, and the order in which the program is to list tasks. The display also gives you several options about screen format. You can change the column width for task names and resources, or alter the length of time shown on the screen.

At the end of the Setup section, the program asks if everything is okay. If you say "No," the software cycles through the entire set of screens to allow you to modify them appropriately. If you select "Yes," you are taken to the Task entry screen.

Task entry

The Task form allows you to add or modify tasks, and to specify their sequence. After entering the task date, you press the Insert key to add the next task. To modify an existing task, you press the F2 key. Task names, limited to thirty characters, must be unique.

A word of caution here. Depending upon the sort routine you set, activities may not follow the logical grouping you expect because of the letter of the alphabet you used. A little preplanning, using "A- " as the first characters in the description block for tasks you want to show in the upper lefthand corner of the Gantt chart, "B- " for the next group, and so on, keeps the Gantt chart sequential.

You can define the type of task. The selection includes Fixed, As Soon As Possible (ASAP), As Late As Possible (ALAP), and Span. Span permits you to bridge the time between two tasks. Selection of Fixed requires the entry of the starting or ending dates of the fixed task. This feature is handy for milestone information and fixed meetings, such as design reviews.

Status is entered using the same data screen as the Current Status block. Future, Started, and Done are the selections that permit you to update the Gantt chart as the project progresses. Time to Complete is an information field that provides the time remaining for the task selected.

The Priority feature only affects the schedule when using Resource Leveling. If Time Line must make a choice between two or more tasks that could be scheduled at the same time, it will calculate which task is scheduled first.

The Summarize feature permits the summarization of lower tiered schedules into a main or master schedule for large, complex projects. It helps you with resource loading and schedule performance for the engineering pool or department.

Who/Cost permits the entry of resources and costs, limited to 12 different units. Commands available to modify entries once made include Edit, Delete, Copy, Go To, Join, Split, and Undo, and a few others. They reduce the data entry time considerably. The Copy feature, for example, duplicates task information and leaves a Task data entry screen with a blank Name when you want to enter a slightly different task.

Dependencies

A schedule is a group of related tasks performed in a defined sequence. With Time Line, you identify tasks using the Task form, and specify their sequence by setting dependencies. A dependency indicates that one task must be completed before another task can begin. The earlier task is called the predecessor, while the later task is referred to as the successor. Each task in the project can have as many dependencies as necessary to show its true relationship to other tasks in the schedule.

Time Line provides for all the traditional relationships—Start to Start, Finish to Start, Finish to Finish, with appropriate Leads and Lags. Several techniques are provided for reviewing dependencies. On the Gantt chart, you move the cursor to the task in question and then press the F7 key. All predecessors and successors will be highlighted on the screen. A similar feature is provided on the PERT chart.

One of the truly innovative features of the software is the way it handles sorting of tasks. You can sort by task start date, task name, or by either of the two note fields on the Task form. You can restrict the number of sort characters by placing a slash (/) between the sorting information and other information in the name or notes fields.

Filtering provides further selection of tasks that have some attributes in common even though they are different activities. There may be several tasks, for example, that share the same resource or are on the critical path that you want to review. Filtering allows you to pick those tasks based on their shared attribute and view them from different perspectives. You can also temporarily hide the tasks that don't match the filters by pressing Shift/F7 and selecting the Hide option.

Reports

Reports are very important because they communicate the status of the project. Time Line's series of reports provide adequate coverage. The program has twelve reports, three graphic and nine tabular. It supports screen, printer, and plotter applications. The Gantt charts and time-phased networks from the plotter are crisp in appearance and the current status is clearly visible. Filter Enhanced graphics automatically boldfaces filtered tasks on the screen and flags them with colored crosshatching on the finished graph.

Tabular reports for resources and costs are presented by resource, by task, and by period. An Actual-vs-Planned report shows the tasks that caused the change in schedule between the planning stage and the actual implementation.

Recommendations

Time Line provides a balanced, straightforward, and relatively inexpensive software package that will work very well for the project engineer or engineering group leader with a small- to moderate-sized group or project to manage. You can easily learn it in an hour or so even if you have had little previous experience with automated project management systems. It is relatively full-featured, providing multiple calendars (days, hours, minutes), resource leveling, comparative schedules (actuals to planned), and several easy-to-read, appropriate reports. The manual is well written and supports the software nicely.

Time Line can be used on a local area network (LAN), although the manual warns that you do so at your own risk. Time Line will also upload to a software package called Open Plan developed by Welcom Software Technologies for those interested in a more full-featured project management system.

Time Line costs $495; Time Line Graphics, $195. The program requires 256 kilobytes of memory, two disk drives, and DOS 2.0 or later. Time Line is a great buy for those who need a simple system that will help them do a better job of identifying project problems and status.

Time Line specifications

Minimum memory	256K
Maximum memory	640K
Tasks per schedule (256K)	50
Tasks per schedule (640K)	1000
Schedule per project	Unlimited
Resources per schedule	Unlimited
Cost categories per schedule	Unlimited
Dependencies per task	Unlimited
Calendars per schedule	1
Resource/costs per task	12

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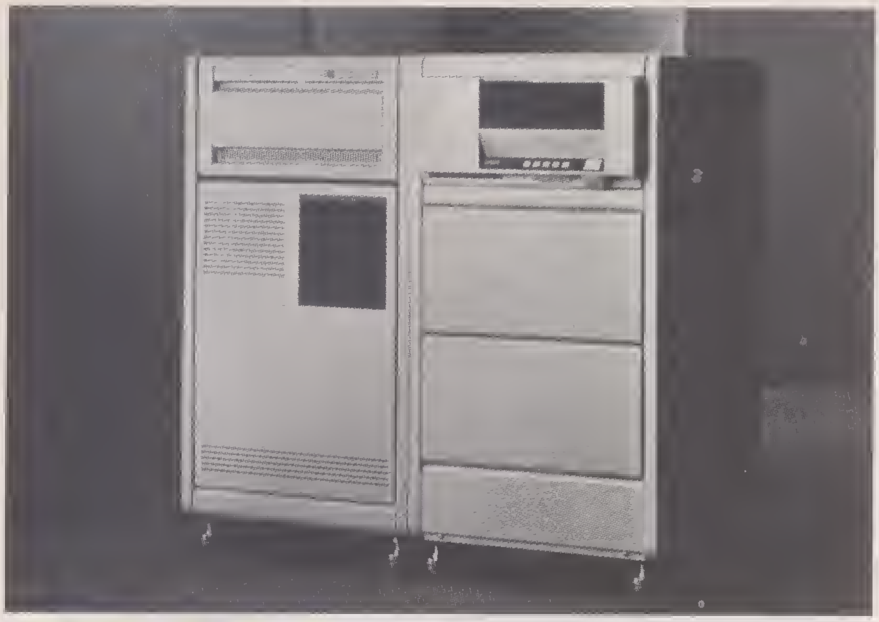
MicroVAX 3600 testing

Neil Baldridge, Compu-Share

The staff at Compu-Share carried out a series of tests to find the maximum number of users supported by a MicroVAX 3600 in a typical commercial environment (based on our own experience).

Our test environment was a Cobol-based transaction processing system. The type of work performed involved a high volume of storage transactions in RMS indexed files, indexed inquiry from the same files, and report generation using keyed as well as sequential I/O.

We used a MicroVAX 3600 with 24 megabytes of memory, an RA82 system device, and an RA81 second disk for all tests. We connected all terminals to the system through Ethernet terminal servers. The disk load was balanced fairly evenly between the two disks. The operating system was VMS version 4.6A. While we did not use a full complement of 32 megabytes of memory, the applications did not page fault excessively during the tests. Of course, if we had used more memory-intensive (or less shareable) applications, additional memory would have been helpful.



The MicroVAX 3600 from Digital Equipment supports up to 100 users, according to the results of a private test.

To obtain reproducible results, we automated the tests by driving all of the jobs from software. We performed six separate tests with the same applications: 10, 20, 40, 60, and 100 simultaneous users. This procedure allowed us to control the delays expected between entering fields, given efficient users. We actually found that the load placed on the system in our software-driven tests was a little heavier than would be expected from human operators.

Despite all the numerical data we collected, our most important measurements were actually made by the users during the test. We evaluated the time required for image activation, record retrieval, and screen form painting—usually the most meaningful indicators of performance to users. We found that we got acceptable responsiveness in the range of 80 users. Beyond this range, we found the response of image activation and other features unacceptably slow.

In our opinion, the MicroVAX 3600 is a phenomenal performer in a commercial environment with Cobol applications. We believe that it can support up to 100 users, since approximately 33 percent of the users on a commercial system are idle at any point in time (and usually remain idle for a few minutes at a time) and our tests did not incorporate any extended periods of idle time.

We must point out that our performance measurements involved our estimate of an "average" situation, based on typical commercial applications and high-volume use. Moreover, we set up our tests to include a high percentage of shareable memory. Obviously, if excessive amounts of physical memory were consumed, fewer users could be supported. Also, all applications involve areas that consume few resources and areas that consume many resources. Our test tended to average out resource consumption and our estimate of 100 users assumes that "average" resource consumption is the rule.

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Powerful word processing

Dick Eckhouse

From its initial introduction to its current incarnation (Version 4.0), Microsoft's Word has been a versatile and feature-packed word processor. With each new version have come additional features (such as spelling and hyphenation, a thesaurus, table and multicolumn output, indexing, outlining, math, and so on), yet the system requirements have remained rather modest: 256 kilobytes, two floppies, and DOS 2.0 or higher. Thus, Word can be used by both the beginner with modest system resources and the sophisticated user with a laser printer and demanding word processing needs.

Two complaints are often heard regarding Microsoft Word. The first is that it is too slow and the second is that it is too complex. Now, in the latest version, both of these complaints have been addressed. First, Version 4.0 of Word is noticeably faster. The system starts up quickly and the cursor moves noticeably faster. Because you can now toggle between text and graphics modes, you can take advantage of the speedier text mode when scrolling through a document, then switch to graphics mode to get a WYSIWYG display.

Second, attention to detail has made Word easier to use. Gone is the dreaded Alpha mode that left the user frustrated when entering commands and text. In addition, cursor keys can select commands; command prompts appear as you scroll through options; borders can be removed; column, line, and page counters keep track of where you are; and a document retrieval system makes it possible to identify a document by a number of categories (such as title, comments, author, operator, date, and so on). Since it is a document retrieval system, you can also perform a search on keywords included with the title, as well as within the document itself.

As a Word owner from the very start, I must admit to thinking that Word is for the "power user." The concept of style sheets, glossaries, and actual display of the formatted text has been both exciting and frightening. Much of the time I put Word aside to use a less powerful system that doesn't offer the same wealth of features and capabilities, but demands much less of me if all I want to do is enter simple text with a few underlines here and a word or two boldface there. Also, my simpler word processor has always maintained its own directory with up to 30-character descriptive titles so that I didn't have to wonder what LETTMKE.DOC really contained. Word's new document retrieval system, its "style by example," and the fact that my simpler system now requires 384 kilobytes have forced me to rethink the earlier decision.

I have long had a love/hate relationship with style sheets. While they are a powerful feature, making it easy to define and redefine what a document looks like, they usually require considerable time to define and test. The new version's "style by example" means that you can now develop a new style, apply it to some text, revise it until it is just what you want, and then save it for future use. What a great improvement for the casual user.

At the opposite extreme are macros, a new Version 4.0 feature. Power users will like the power they offer, and casual users may find the canned ones provided with the software both useful and intriguing (like generating a concordance-based index). I liked the example included with the reviewer's guide, which generated memos, letters with envelope addressing, and other useful "office procedure" types of forms. The one for filling out an expense report is sure to please anyone who has written a similar document using a spreadsheet.

Speaking of spreadsheets, Version 4.0 also includes a spreadsheet link to Lotus and Multiplan. While the link is handy, using hidden text to link to the cells in the spreadsheet so that changes in the spreadsheet data are reflected in the Word document, it is not an easy tool to use. One reason is that setting up the link is not as easy as just highlighting a set of rows and columns, as you might do in some other system. A second reason is that, having brought in the spreadsheet data, you need to format the columns (width, number of columns, and alignment). While the example on the review disk included a macro to do this, the more generalized case may require some effort.

Two other new features in Version 4.0 are paragraph borders and line drawing capabilities, and red-lining and revision marks. Both are nice to have, but are not as important to me as the features already described.

A few things in the last version that I did not care for remain in the current version. First, the spell checker is clumsy, showing only a few lines of surrounding text and not correcting text in place. Second, the use of Shift-Return instead of just Return for an inside address is cumbersome. Finally, the function, Alternate, Control, and Shift key combinations of the last version were already difficult to remember. Now there are even more of them. True, the new templates help, but I must admit to still being intimidated. However, I keep and use Word for all the tough tasks that my simple word processor can't handle.

Included with my package were both 5¼-inch floppies and the newer 3½-inch floppies, a reference manual, and an excellent printer support manual in case your printer isn't among the 100 or so supported. A flyer from Microsoft lists a large number of companion products that offer additional features like the inclusion of graphic images, mathematical typesetting, and laser printer font support.

Microsoft Word Version 4.0 costs $450, with an $75 upgrade offer to registered users of Version 3.x.

Reader Service 27

Excellent, low-priced CAD

Dick Eckhouse

Like word processors, mechanical computer-aided design systems are now available in abundance. It's likely that once you've used one, all others will be measured against it. Thus, if you've latched onto something you like, stay with it; if you haven't, let me recommend a low-priced yet complete and powerful CAD program to try.

I won't go into the same level of detail that I did when I reviewed Generic CADD in the March 1987 issue of *IEEE Software*. However, I'd like to point out that the folks at Generic Software have been busy. Their recently released version 3.0 is billed as 20 percent faster, with more user control and more accurate screen displays.

Since CADD 2.0 was no slouch when it came to speed, I will ignore the speed aspect in this review. Let me point out instead what I find really attractive, namely, an outstanding new manual, more (displayable) line types and views, and a hatch/fill capability not found on systems selling for considerably more. Let's take a look at each in turn.

First is the manual. I am a bug on well-written manuals because they are so important in understanding and using complex software. They should include a good index; a tutorial; an explanation of the overall system and how it functions, plus necessary details for the knowledgeable user; a description of all commands; and lots of examples to clarify the concept(s) presented. In this regard the latest version of Generic CADD really shines. Not only does it address all these points, but the organization makes it easy to find needed references. Marginal notes highlighting the concepts presented makes scanning for information very fast.

The first chapter in the manual addresses all the issues, from system requirements to manual organization, a definition of CAD, and naming of system files. The second chapter fills you in on using Generic CADD, while the third is a tutorial, helpful but possibly too brief if you're really inexperienced in CAD systems. The next chapter covers all the commands thoroughly, including appropriate figures for most. The appendices cover menus, batch files, installation, configuration, and fonts.

Obviously, I'm impressed with Generic's thoroughness. Another feature I liked is that the manual is designed to accept additional modules (such as drafting enhancements, auto dimensioning, DotPlot, etc.) as you buy them, so that you have all the reference materials in one place.

Second are the line types and views. Of the up to 256 line types, the first 10 appear on the selection menu; the remaining sets represent scaled versions of them. Color selection for lines is also through a menu, so that you can choose from the actual screen color. You can select one of 10 line widths. The on-screen lines are then drawn according to your selection.

Another feature of version 3.0 is named Views. This feature allows you to name the currently displayed view so that you can later return to the view with the zoom command. Thus, you need not zoom out and in to move from one part of a drawing to another.

The third new feature is Hatching and Fills. This feature is only available if you purchase the DE-2, or Drafting Enhancements-2, module. DE-2 includes 16 hatch patterns, the ability to fill with any displayable color, and the potential to create your own hatch patterns using a word processor or text editor. The module integrates well with the base system, having the same philosophy of allowing the user to change display variables (like color, size, rotation angle, etc.) to customize the end result.

DE-2 costs $50, as do the other optional modules. Given the low price of the base system, plus the functionality offered with the additional modules, my recommendation is to buy them all. For $300 you will acquire a very complete system at about one-tenth the price you'd have to pay for one of the well-known alternatives.

Generic plans to offer a new set of 3D programs for the construction of solid model representations of any object in a wireframe display. Generic 3.D Solids Modeling will sell for $200 and the Rendering Module, for $150. The base price for Generic CADD remains $100.

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NEW PRODUCTS

Microsoft Windows/386 taps 80386 capabilities

Microsoft offers a new version of the Windows operating environment for Intel 80386-based personal computers, called Microsoft Windows/386. According to the company, the new product provides multitasking, expanded memory support, 640K-byte virtual machine support for existing MS-DOS applications, memory management for Windows applications, and visual compatibility with the Microsoft Operating System/2 Presentation Manager being developed with IBM.

Windows/386 was developed with Compaq Computer.

Besides allowing users to run multiple applications at once, the software reportedly allows users to run existing MS-DOS applications in a window alongside Windows applications.

Windows/386 runs on the Compaq Deskpro 386 and compatibles, as well as the IBM PS/2 Model 80. An original equipment manufacturer version is available for other 80386-based computers. The company recommends 2M bytes of physical memory. The system requires a hard disk and an EGA or VGA display adapter. The user interface was reportedly designed for use with a mouse, but does not require it.

Windows/386 costs $195, with an upgrade available to registered Windows 1.0 users for $95.

Reader Service 30

New Compaq portable and PC employ 20-MHz 80386

Compaq Computer has announced the Compaq Portable 386 and the Compaq Deskpro 386/20, based on the 20-MHz Intel 80386 microprocessor.

The Compaq Portable 386 starts at 20 pounds. It features up to 10M bytes of 32-bit RAM, up to 100M bytes of hard disk storage, a 1.2M-byte disk drive, an optional 20-MHz 80387 coprocessor, and an optional expansion unit.

The Compaq Deskpro 386/20 (left) and Portable 386 (right) use the 20-MHz Intel 80386 microprocessor to attain what the company claims are significantly faster processing speeds.

Other options for the Portable 386 include a 40M-byte tape expansion unit and 1200-baud or 2400-baud Hayes-compatible internal modems.

The Compaq Portable 386 operates with MS-DOS Version 3.2 and later. Model 40, which features a 40M-byte hard disk drive, costs $7999. Model 100, which features a 100M-byte hard disk drive, costs $9999.

The Compaq Deskpro 386/20 incorporates the company's Flex architecture (Flexible Advanced Systems Architecture), which combines a memory caching scheme with a concurrent memory and I/O bus. It also features the Intel 82385 cache memory controller, up to 300M bytes of hard disk storage, and up to 16M bytes of 32-bit RAM.

The Deskpro 386/20 Model 60, which features a 60M-byte hard disk drive, costs $7499. Model 130, which features a 130M-byte hard disk drive, costs $9499. Model 300, which features a 300M-byte hard disk drive, costs $12,499.

Compaq will include Microsoft Windows/386 with all Deskpro 386/20, Portable 386, and Deskpro 386 computers shipped by December 31, 1987.

Portable 386: **Reader Service 31**
Deskpro 386/20: **Reader Service 32**

Excel adds spreadsheet to Windows

Microsoft has announced the Excel spreadsheet for Microsoft Windows. Based on Excel for the Macintosh, the new version reportedly provides dynamic linking of spreadsheets, an automatic macro recorder, and high-resolution printed output. It also features integrated database management and customizable graphs.

The company says it designed Excel for Intel 80286- and 80386-based personal computers. The product runs under Windows 2.0 and Windows/386, and will be available for OS/2 (with an upgrade price of $50 for Excel users).

Microsoft claims to have built in a bridge from Lotus 1-2-3, including two-way file compatibility, learning tools, and a 1-2-3 Macro Translation Assistant.

The Excel spreadsheet measures 256 columns by 16,384 rows.

Excel runs on the IBM Personal System/2, Compaq Deskpro 386, or compatibles. It requires 640K bytes of memory, MS-DOS 3.0 or higher, a hard disk drive, and a graphics adapter card. It costs $495. Current users of Multiplan can upgrade for $250.

The Windows interface is reportedly identical to that of Microsoft OS/2 with Presentation Manager. Registered users of Excel will be able to upgrade to the OS/2 environment for $50.

For $995, users whose machines don't meet the above requirements can get Excel, a Microsoft Mach 20, and a Memory Plus board.

After installation of Excel on a network server, a company can purchase Workstation User Manual Packs for $250 each.

Reader Service 33

Works combines applications for DOS-based systems

Microsoft has announced a version of Works for the IBM PC and compatibles and the IBM Personal System/2. The software reportedly targets home and small business users, combining a word processor, spreadsheet with charting, database with reporting, and communications module.

The software also features macros that span all the application modules, the ability to print mixed text and graphics, a choice of character fonts, and charting. According to the company, users can have multiple documents of different types, such as a spreadsheet and a letter, open at the same time.

Microsoft Works for the PC reputedly offers file compatibility with higher-end products such as Microsoft Word and Lotus 1-2-3, permitting transfer of files.

The program, which targets first-time users, costs $195. It requires 384K bytes of memory and either two 360K-byte disk drives, one 720K-byte disk drive, or a hard disk drive. The package comes with both 3½-inch and 5¼-inch floppy disks. To display graphics or charting, Works requires a CGA, EGA, or Hercules graphics card.

Reader Service 34

Micropro upgrades Wordstar, offers personal and legal editions

Micropro International has upgraded Wordstar to Wordstar 2000 Plus Release 3 and offers two software programs based on the core word processor. Personal Edition targets general office users and Legal Edition, legal users.

Personal Edition includes programs to create presentations, fill in preprinted forms, and organize outlines. It costs $495.

Legal Edition includes programs to compare document drafts, check citations, and fill in forms, plus a legal dictionary. It costs $595.

Both versions come with 3½-inch and 5¼-inch floppy disks for IBM personal computers and compatibles. Registered users of Wordstar can purchase either version with the core program for $149, or the core program alone for $89. Local area network update pricing is $89 for the server and $30 per node.

Personal Edition: **Reader Service 35**
Legal Edition: **Reader Service 36**

WORM drive targets OEMs

Laser Magnetic Storage International has announced the Laserdrive 510, a 654M-byte write-once read-many times optical disk drive.

According to the company, the WORM drive targets original equipment manufacturers and systems integrators. It offers 327M bytes of storage per side of a double-sided disk and reputedly achieves a 600K-byte sustained transfer rate, an average access time of 75 ms, and a maximum track-to-track seek time of 1.5 ms. Interfacing is handled through an embedded small computer system interface.

The LMS Laserdrive 510 costs $2880; media costs $95.

Reader Service 37

Optical system with DB

Skan Teknologies offers the Arkive/CRS optical disk subsystem, which the company claims works in conjunction with a database to allow a mainframe to communicate directly with the optical disk. The system operates either as a node of a mainframe, or as a stand-alone system.

System capacity ranges from 1G byte up to 4.2T bytes. Media capacity ranges from 1M byte to 3.2G bytes per disk, with prices depending on capacity. Media are manufactured by Sony, Optotech, and Optimum.

Pricing for thc Arkive/CRS system starts at $30,000.

Reader Service 38

New optical system for PCs

Optisys offers the MMi-100 Optidriver for the IBM PC and compatibles using MS-DOS. The stand-alone system combines hardware and software in an optical storage disk drive that uses 400M-byte cartridges costing $200 each.

According to the company, the system is SCSI compatible and DOS transparent. It reputedly achieves an average access time of about 80 ms and a transfer rate of 90K bytes per second.

Optisys claims that the system installs in around 15 minutes, requires no additional training to use, and works with most software packages.

The MMi-100 Optidriver costs $4995.

Reader Service 39

LAN operating system for IBM introduced

Western Digital has announced Vianet Professional, a local area network operating system compatible with IBM standard commands and protocols and targeting original equipment manufacturers.

The operating system supports the IBM PC, PC-XT, PC-AT, PS/2, and compatibles running PC-DOS or MS-DOS Version 3.10 or later. It operates with LAN adapters using Netbios protocols, including Western Digital's WD8000 and WD8003S Starlan and WD8003E Ethernet products, and the IBM PC Network and Token-Ring adapters.

The program features pull-down menus and automated network administration, according to the company, as well as a Unix-like security system. It is compatible with the IBM PC LAN Program and Microsoft Networks (MS-Nets). A menu-driven installation program reputedly permits a user to configure, add, or remove nodes and resources without interrupting the network. The software also has on-line diagnostics.

Vianet Professional costs $150.

Reader Service 40

Sony offers new internal & stand-alone optical drives

Sony's Optical Memory Group has announced the CDU-510, an internal half-height CD-ROM drive, and the MPX Series of stand-alone CD-ROM drives. The drives target original equipment manufacturers.

The CDU-510 has an IBM PC, PC-XT, and PC-AT interface. It uses the Sony standard CD-ROM cartridge.

The MPX Series consists of four models. Two of the drives (models MPX-601 and MPX-602) feature an IBM PC, PC-XT, and PC-AT interface, with one of the two having audio capability. The other two drives (models MPX-603 and MPX-604) feature an SCSI interface, one of them with audio capability. All four use the Sony standard CD-ROM cartridge.

All of the new drives reputedly achieve a transfer rate of 153K bits per second and an average access time of around 500 ms. They use standard media with storage capacity of 660M bytes per disk.

The CDU-510 costs $540. Prices for the MPX Series range from $680 to $970.

CDU-510: **Reader Service 41**
MPX Series: **Reader Service 42**

Emerald offers WORM drive, tape backup systems

Emerald Systems has announced two new product lines: the DOS 400-10030 optical disk drive, and the DOS 60-9007 and DOS 150-9007 tape backup systems for the IBM Personal System/2 Series, Models 50, 60, and 80.

The DOS 400-10030 is a write-once read-many times random access storage device with up to 200M bytes of capacity on each side of a removable cartridge, according to the company. It is reportedly designed for use as an external drive with the IBM PC, PC-XT, or PC-AT; Compaq Deskpro 286 or 386; and compatibles.

The WORM drive employs Emerald's proprietary error correction codes to achieve what the company claims are error rates of less than one in 10^{12}.

Emerald's DOS optical disk drives come with two device drivers: the standard DOS interface and the customizable File Management System.

The DOS 400-10030 optical disk drive costs $3995.

The PS/2 subsystem models include the tape drive in a self-contained external chassis with power supply and an adapter board that fits in an open slot on the Micro Channel Bus. Another adapter board and cable modify the systems for use with the IBM PC, PC-XT, and PC-AT.

The DOS 60-9007 is a 60M-byte unit and the DOS 150-9007 is a 150M-byte unit. The DOS 300-11007 is a 300M-byte unit that comes in a larger chassis containing two 150M-byte tape units.

The DOS 60-9007 costs $2395; the DOS 150-9007, $3295; and the DOS 300-11007, $6395.

WORM drive: **Reader Service 43**
PS/2 units: **Reader Service 44**

Tandem launches WORM for Nonstops

Tandem Computers has announced a write-once read-many times optical disk library system called the 5200 Optical Storage Facility for use with Tandem Nonstop computer systems.

The 5200 contains two read/write disk drives, a formatter, and an automatic changer for up to 32 disk cartridges. Each 12-inch cartridge holds 2.62G bytes of data, for a total of 84G bytes of storage.

The storage system works with the Tandem Nonstop VLX, TXP, Nonstop II, EXT25, and EXT10 systems. It reputedly achieves an average access time of 250 ms for data on an already mounted cartridge, and 17 seconds when a cartridge must be changed.

The 5200 Optical Storage Facility, including the automatic changer, two disk drives, control unit, and cables, costs $155,000. The software initial license fee is $5300 and the monthly license fee is $100 for the Nonstop VLS, TXP, Nonstop II, and EXT25 systems. The fees are $2650 and $50, respectively, for the Nonstop EXT10 system.

Reader Service 45

Automated system tests optical media

California Peripherals (Caliper) has announced an optical media tester called the Caliper OMS-2000.

According to the company, the system tests formatted and unformatted media at spindle rotation speeds of up to 3600 revolutions per minute. It reportedly evaluates each track, as well as preformatted sector data as proposed by ISO standards.

The OMS-2000 evaluates magneto-optical, write-once, and phase-change media, in continuous or sample servo formats of all three standard sizes. It measures optimum read, write, and erase performance; carrier-to-noise ratio; harmonic content; the noise level of the fundamental signal; media reflectivity; media reliability; preformatted data; and jitter, drop-in, and drop-out.

The system includes an optical drive unit, drive controller, system controller, software, terminal, and optional printer for about $225,000. The OMS-2000 will be available in the first quarter of 1988, with volume production scheduled for the second quarter.

Reader Service 46

Software helps WORM drives blend in with DOS devices

Information Storage has announced a software package called WORM-TOS (Transparent Optical Software) to help its write-once read-many subsystems blend in with standard DOS devices.

WORM-TOS reputedly supports all DOS features, including subdirectory trees; renaming, deleting, or appending files; selective file alteration; and so forth. It also allows direct access to the optical disk using standard DOS commands.

An ISi 525 WC optical disk subsystem for internal mount in an IBM PC, PC-XT, PC-AT, or compatible systems with WORM-TOS software costs $2595. An external-mount optical disk subsystem including cabinet, drive, controller card, WORM-TOS software, and cable costs $2795.

Reader Service 47

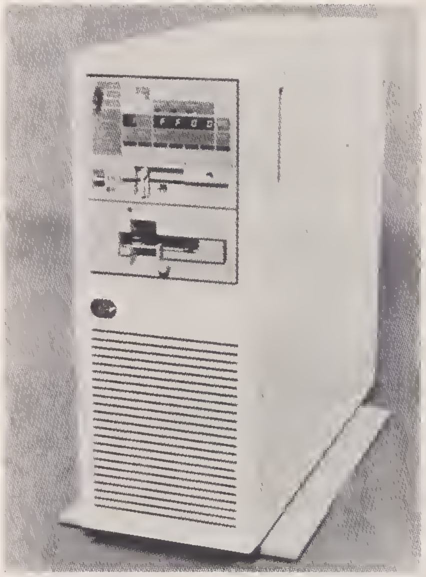
IBM expands System/36 with entry-level model

IBM has announced an entry-level model in its System/36 computer family. The company offers the System/36 5363 System Unit as a preconfigured System/36 Total System Package with preloaded operating system software. The TSP also includes selected displays and printer, optional office application software, and supplies.

Standard features include one megabyte of main storage, a System/36 format-compatible 1.2M-byte disk drive, addressability for up to 16 local and 64 remote displays or printers, 65M bytes (Model P10) or 105M bytes (Model P20) of integrated disk storage capacity, and a variety of expansion options.

The 5363 Model P10 costs $10,995 with preloaded OS and $10,000 without. The 5363 Model P20 costs $12,095 with preloaded OS and $11,100 without.

Reader Service 48



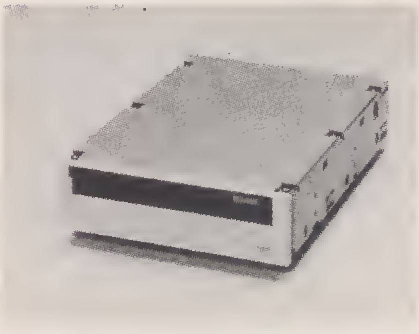
The IBM System/36 5363 System Unit is a floor unit that does not require a PC as a console because it houses its own feature cards.

CD-ROM averages 400-ms access time

Toshiba America has introduced the XM-3100B CD-ROM optical disk drive, which the company claims has an average access time of 400 ms. The half-height drive accepts industry-standard CD-ROM cartridges holding 680M bytes. It features audio capability and an embedded SCSI interface.

The XM-3100B costs under $600 in OEM quantities over 100 units.

Reader Service 49



Toshiba America's XM-3100B half-high CD-ROM disk drive targets the OEM/VAD/VAR market.

OCR "learns" new typestyles

Advanced Recognition Technologies has announced the Smart Start optical character recognition software program for the IBM PC, PC-XT, PC-AT, and compatibles. The software outputs digitized images as ASCII code or as a formatted file for word processing and desktop publishing software programs that accept ASCII files.

According to the company, the name Smart Start comes from "self teaching advanced recognition technology." The program reputedly is capable of "learning" any 6- to 14-point typestyle.

Smart Start comes with monospace, proportional, and typeset fonts. A user can reputedly specify the areas of a page to be read, excluding unwanted text, graphics, and so forth.

The software requires machines with 512K bytes of RAM; PC-DOS or MS-DOS; and a Hercules, CGA, or EGA graphics card. The company recommends a hard disk.

Smart Start costs $495.

Reader Service 50

Gateway links IBM machines and Decnet networks

Interlink Computer Sciences has announced the 3732 Gateway (model 400), a 32-bit gateway linking IBM mainframes and Decnet networks.

The 3732 Gateway is based on Digital Equipment's MicroVAX II and uses DEC's MicroVMS operating system. It implements Interlink's communications architecture, Network Port Architecture. According to the company, NPA allows adding new components for future connection to other networks, such as TCP/IP, MAP, and OSI.

The gateway reputedly handles data throughput rates of up to 800K bits per second and supports up to 128 simultaneous sessions.

Like other Interlink gateway products, the 3732 connects IBM or compatible mainframes into Decnet as peer nodes. The master software resides on the mainframe and runs as an application.

The combined hardware and software product costs $69,950.

Reader Service 51

IC Announcements

Company, Model, Function	Comments	R.S. No.
Analog Devices AD7245, AD7248 DACs	Monolithic 12-bit D/A converters with on-chip output amplifier and voltage reference. Feature 5-μs settling time and power dissipation of 135 mW. AD7245 accepts data in a 12-bit broadside format; AD7248 provides an 8 + 4-bit interface for 8-bit buses. Available in 24-pin DIP, LCC, and PLCC over three temperature ranges. Cost: starts at $9.85 (100s).	120
Analog Devices AD7579, AD7580 ADCs	10-bit sampling A/D converters. Perform a conversion in 20 μs and feature 25-KHz input signal bandwidth. AD7579 loads in a 8 + 2 format; AD7580 loads with one 10-bit parallel word. Available in 24-pin plastic or ceramic DIP, or 28-lead LCCC/PLCC over three temperature ranges. Cost: starts at $9 (100s).	121
Burr-Brown AD632 Multiplier	A monolithic multiplier with on-chip reference, multiplier core, and precision output op amp. Alternate source for the four-quadrant analog multiplier of the same number. Available in hermetic metal TO-100 and 14-pin cerdip packaging over two temperature ranges. Cost: starts at $9.90 (100s).	122
Intech Advanced Analog ADC1140 ADC	A 16-bit successive approximation A/D converter with a 35-μs conversion time. Consumes 1.6 mW from ±12V to ±17V. Accepts analog input signals either unipolar from 0 to 10V or bipolar from 5V to ±10V. Operates over −25° to 85°C. Cost: $151 (lots of 100).	123
Integrated Device Technology IDT75C48 ADC	An A/D converter pin- and function-compatible with the TRW TDC1048 bipolar device, but with power consumption of 500 mW. Includes on-chip error detection and correction. Comes in 28-pin plastic, DIP, cerdip, or LCC. Cost: $75 (100s) for commercial grade plastic DIP.	124
Micro Networks MN6290, MN6291 ADCs	16-bit sampling A/D converters with track-hold amplifiers and sampling rates up to 20 KHz. Target digital signal processing applications. MN6290 has a 10V input span and MN6291, a 20V input span. Both come in two electrical grades and over two temperature ranges. Cost: starts at $180 (100s).	125
Motorola MC68HC05L6 Microcomputer	An 8-bit microcomputer with on-chip liquid crystal display driver, oscillator, CPU, 6208 bytes of ROM, 176 bytes of RAM, serial peripheral interface, 16-bit timer, and audio tone generator. Available in die form only; packaged samples come in a 68-lead PLCC. Cost: $12.95, minimum 1000 units, plus $5300 mask charge.	126
Motorola MC145402 D/A & A/D converter	A serial 13-bit linear monotonic D/A and A/D converter. Features on-chip voltage reference and typical 60-dB signal to noise and distortion. Power consumption of 40 mW, 1 mW power down. Available in a 16-pin cerdip. Cost: $7.67 (1000s).	127
Tektronix TKAD20C ADC	An 8-bit A/D converter from DC to 125 MHz. Features input signal bandwidths up to 2.3 GHz, on-chip track and hold, and selectable demultiplexed output. Uses ±5V power supplies and dissipates 5W typically. Comes in an 84-pin ceramic package. Cost: $850 for the commercial version.	128
Texas Instruments SN74ACT29116, SN74ACT29166-1 Processors	Microprogrammable, 16-bit processors. Pin-compatible with the Am29116, but consume 145 mW at 10 MHz and 30 μW in standby mode. Operate over the temperature range 0° to 70°C. Come in a 52-pin cerdip and a 64-pin PLCC. Cost: $50.40 (1000s) for the 74ACT29116; $62.50 (1000s) for the 74ACT29116-1.	129
VTC VA730 Amplifier	A monolithic sample and hold amplifier that operates at 75 MHz with 9-bit accuracy using ±5V power supplies. Compatible with surface-mount technology. Comes in a 20-pin CLCC and LCC and 14-pin cerdip. Available in commercial and military versions and in die form. Cost: $14.25 (100s) for the 14-pin version, $20.35 (100s) for the 20-pin version.	130
VTC VC512 DAC	A bipolar, 12-bit multiplying D/A converter. Features ±½ LSB maximum differential nonlinearity with 13-bit accuracy and a settling time of 125 ns. Delivers an 8-milliamp output. Operates with ±5V power supplies. Comes in a 28-pin LCC and PLCC, 24-pin SOIC, and 22-pin and 24-pin DIPs. Available in commercial, military, and die forms. Cost: ranges from $38.70 for plastic packages to $125 for surface mount military packages (100s).	131

Microsystem Announcements

Company, Model, Function	Comments	R.S. No.
Case Communications Case 208A/B Modem	A 4800 bps dual-mode synchronous modem. Operates full-duplex over leased transmission lines and half-duplex over leased or dial-up public lines. Monitors signal quality and automatically recalibrates the connection. Compatible with Bell and Case 208 modems. Comes stand-alone or rack-mounted. Cost: $1195.	135
Concord Data Systems 296 Trellis Modem	A 9600/4800-bps, full-duplex, asynchronous/synchronous modem compatible with the CCITT V.32 standard. Features two-wire dial- and leased-line communications, MNP class 4 error correction, and remote modem configuration capabilities, including the Concord command set, Hayes AT-compatible mode, and V.25 bis dialing. Cost: $1795.	136
Control Data Swift family 3½-inch drives	Includes eight models ranging from 55M bytes to 200M bytes, with 16.5- or 25-ms average seek times. Supports the common command set of instructions for the SCSI interface. Comes with ESD1, SCSI, and ST506 interfaces. Claims a mean time between failure of 30,000 hours. Evaluation units available first quarter 1988. Cost: about $6 per Mbyte.	137
Dyna Computer SX386 Motherboard	An 80386-based motherboard for the IBM PC-XT and compatibles. Includes an Intel 80386 microprocessor, four 16-bit and four 8-bit I/O slots, 16-MHz memory bus with 32-bit addressing, 2M-byte DRAM modules (expandable to 8M bytes), and support for Intel 80287 and 80387 math coprocessors. Cost: $1650.	138
Edge Computer 2000 Series Superminicomputer	A VME board set making up a 68000-compatible superminicomputer. Available in four versions accommodating from 500 to 1000 users: Model 2100—single processor, 16 MIPS sustained and 22 MIPS peak performance; Model 2200—dual processor, 30 MIPS and 44 MIPS; Model 2300—triple processor, 43 MIPS and 66 MIPS; Model 2400—quad processor, 55 MIPS and 88 MIPS. Cost: starts at $25,000 OEM.	139
Force Computers CPU-29 CPU	A single-board CPU with 32-bit VMEbus and VME subsystem bus interfaces. Based on VME/Plus architecture and the 68020 microprocessor. Available in three versions, with clock rates of 12.5 (CPU-29XS), 16.7 (CPU-29X), and 25 (CPU-29B) MHz. Comes with VMEPROM operating system kernel and Forcebug monitor/debugger software, plus 1M-byte 100-ns SRAM. Cost: $2990 (CPU-29XS), $3990 (CPU-29X), $6390 (CPU-29B).	140
Hercules Computer Technology Network Card Plus Graphics/LAN board	A PC add-in board combining high-resolution graphics with an Appletalk network port. Incorporates the features of the Hercules Graphics Card Plus, including 720 × 348-pixel resolution and Ramfont. Networks with PCs, Apple Macintoshes, and Unix-based systems. Networking software, TOPS/DOS, from codeveloper TOPS. No price given.	141
QMS QMS-PS 810 Laser printer	A Canon SX engine-based laser printer that supports the Adobe Postscript page description language. Employs ASAP (Advanced System Architecture for Postscript) controller technology, which includes 2M bytes of RAM expandable to 3M bytes, 1M byte of ROM, and 16-MHz 68000 MPU. Operates at an 8-ppm speed. Cost: $5495.	142
RasterOps Colorboard 1/104 Graphics board	A graphics board for the Apple Macintosh II. Features 1024 × 768-pixel resolution on a 24-bit color plane that can display 16.7 million colors simultaneously. Pixel frequency of 60 MHz. Initially targets Macintosh II OEMs, VARs, and distributors. Cost: $2795.	143
Strawberry Tree Computers Analog Connection Acquisition & control boards	Eight acquisition and control boards for the Apple Macintosh II and SE. Six boards for the Macintosh II offer up to 16-bit resolution with up to 16 analog input channels, 16 digital I/O lines, and optional analog output channels. Two boards for the Macintosh SE offer 16-bit and 12-bit resolution with 8 channels for analog input of digital I/O. Cost: ranges from $795 to $1845.	144
Thomas-Conrad TC6046 ARC-Card/MC ARCnet interface board	Allows networking of IBM Personal System/2 Micro Channel computers to the ARCnet token-passing LAN. Features a dual-port 2K-byte data buffer and 8K-byte PROM socket for auto-boot PROM installation. Uses 16K bytes of memory address space. Requires no switch settings. Compatible with Novell Netware. Cost: $549.	145
XMIT xGate 100 Series Networking boards	Five X.25 concentrators using the same main board to provide X.25 network access for up to 24 IBM control units. 150T and 150H provide IBM SNA remote and host support, respectively. 144T and 144H supply 3270 remote support. 148 gives 2770/3780 BSC support. Cost: $2500; $1000 for memory extension and expansion module options.	146

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How Pacific nations achieved technological success outlined at FJCC

Harry Mathis, Texas A&M University

Links among research universities, industries, and government, as well as concentration on long-term ventures, have enabled countries in the western Pacific to dominate a technology and achieve long-term returns in technical development.

The nations, particularly Taiwan, Japan, Korea, Hong Kong, and Singapore, recognized that short-term ventures would result only in short-term returns because competitors could quickly enter the market and reduce profitability.

So stated Irving Ho of Taiwan's Institute for Information Industry when he presented the opening address of the October 25-29 Fall Joint Computer Conference in Dallas. Ho delivered the speech for K.T. Li, who was scheduled to appear but was ill. Li is senior minister without portfolio from Taiwan.

Stephen Szygenda of the University of Texas at Austin was conference chair; with Raymond Yeh, Syscorp International, and C. V. Ramamoorthy, University of California at Berkeley, the program chairs; and Toni Shetler, TRW Federal Systems Group, the professional development chair.

Ho outlined the stages of economic development the western Pacific countries underwent to attain their strong present-day technological positions.

First, in the 1950s, government programs that fostered basic industries enabled a reduction in imports, a process Ho called "import substitution." The second stage, characterized by Ho as "export promotion," occurred during the 1960s. In it, further growth was made possible by foreign investment, and exports were promoted through the creation of export processing zones.

The third stage, "infrastructure improvement," occurred during the 1970s. It featured improved transportation and communications facilities and evolved concurrently with the introduction and application of traditional science and technology programs throughout industry.

The fourth stage, the restructuring of industry to take advantage of the latest technology, is now occurring and has become necessary because the countries have lost the advantage of low labor costs, Ho said.

Keynote address. Max D. Hopper, senior vice president of information systems for American Airlines, delivered the conference's keynote address: "Choices Faced in the Strategic Use of Computer Services."

Hopper said he has been seeing "a system-error message flashing on screens across America." He listed some of the reasons for his alarm, saying that (1) 30 percent of America's high schools offer no physics; (2) the scientific knowledge of American students has declined steadily since the 1960s; (3) industry is attracting science and engineering PhDs at twice the rate of academia; (4) the ratio of the US total population engaged in science and engineering has declined compared to the country's key trading partners; (5) America's key trading partners have been achieving productivity increases from five to nine times greater than it has; (6) the Japanese now have a higher average income than Americans; (7) if current trends continue, US workers entering the work force today will have a lower average income at retirement than their counterparts in Taiwan and Korea; and (8) nearly two-thirds of America's record trade deficit is with the Pacific Rim countries (enumerated by Ho earlier) that are using technology developed in the US.

"We must do a much better job of connecting science and technology to our everyday world of education and business," Hopper stated. "If we do not, we risk a future where growth is stunted and the gap widens between the US and other nations, where progress is driven by scientific advancement and technological innovation."

He cited the work of Nobel Prize winner Robert Solow of MIT, which demonstrated how long-term economic growth depends on technological progress, and pointed out that knowledge, embodied in new machines and improved human skills, is the critical element accounting for more than half of all economic growth.

Hopper said that most of the productivity gains in US manufacturing in the 1980s have resulted from closing inefficient plants and applying technology to the assembly line, but that industry

The last FJCC

Paid attendance at the 1987 Fall Joint Computer Conference was 700, barely 56 percent of the 1250 paid attendees budgeted. This marked the second year of the conference's two-year lifespan, begun last year as a joint effort by the Computer Society and the ACM. Last year's conference drew 1400 paid attendees, vs. 2000 budgeted. Exhibitor booth sales reflected a similar pattern: This year's conference was budgeted at 80 10-foot by 10-foot booths but in fact sold only 33. Last year booth sales were budgeted at 200, but actual sales were only 125. Following these two successive years of under-budget performance, the Computer Society Board of Governors and ACM Council voted in Dallas to cancel FJCC 88 and its successors.

The announcement in no way negates the basic agreement under which the conference was initiated, according to Computer Society Conferences Vice President Jim Aylor of the University of Virginia. Other events may well be launched under the agreement by the two societies, and in fact the presidents of both organizations are to meet during the coming months to review new potential ACM-CS joint ventures.

should concentrate on total computer-aided manufacturing environments rather than improving the assembly line.

The service sector, which comprises three-fourths of the US economy, has even more serious problems, said Hopper. Recently, annual productivity gains have been recorded only in tenths of a percent, and part of the problem has resulted from business looking at technology as a support tool rather than a strategic asset.

He quoted Solow as saying, "If someone landed from Mars or, more to the point, from Tokyo, he'd conclude that the computer has had essentially no impact on our white-collar productivity."

If changes are not made, international competition will take over the US service sector just as it has taken over large parts of the country's manufacturing sector, Hopper said.

He proposed a new model, characterized by decentralization and increased connectivity, for the information-based organization of the future. For universities, this will mean greater accessibility to information for students and a strong emphasis on teaching students to understand technology. For businesses, it will mean increased use of interconnected data networks and greater consumer interaction with business technology. As a consequence, business problem-solvers will have to be technicians and managers rolled into one.

Hopper predicted the volume of knowledge will quadruple and, due to today's low population growth rates, the US work force will be much smaller by the year 2000. Thus, the proper use of technology is becoming critically important, he said.

Technical program. The technical sessions were sparsely attended (see box on facing page) despite the fact that, at most, only five of the eight tracks had sessions in progress at the same time.

The papers presented in the software track sessions dealt with topics such as automatic programming, very high level specification languages, software reuse, object-oriented programming, prototyping, difficulties with large software development efforts, and the use of artificial intelligence in software engineering.

The sessions devoted to the difficulties associated with large software development efforts outlined problems related to the Strategic Defense Initiative and the modernization of the FAA's Air Traffic Control System. Another topic that came up several times involved difficulties in verifying and validating knowledge-based software systems.

Two panelists who spoke at one of the evening sessions, devoted to expert systems, were extremely knowledgeable and articulate.

In outlining the need for software engineering of expert systems, Nancy Martin of SoftPert Systems recommended that a phased life cycle be used, that an explicit specification model be created, that a standard design model, such as the classification or configuration model, be utilized, and that knowledge acquisition be driven by the first three, along with well-defined knowledge acquisition processes.

Artie Briggs of Texas Instruments said that verification and validation of expert system software is extremely difficult and that testing is not a substitute. He also stated that rapid prototyping does not negate the need for the sound engineering of systems.

Martin, replying to a question on how to choose between an expert system and a conventional high-level language program for an application, said, "We should not choose the technology first and then force the application into the technology, but perform a thorough analysis of the application and then select the technology."

In a significant paper presented during the AI applications session, Dan St. Clair, professor at the University of Missouri, Rolla, who is currently on leave at McDonnell Douglas Research Laboratories, outlined a working system that incorporates adaptive learning.

The friendship and comradery among what Roger Bates of Texas Instruments called "the elder statesmen of software engineering," was apparent during the final panel discussion on AI and software engineering. Bates reiterated what Martin had stated the previous evening: that software engineering ideas have not yet penetrated AI.

Win Royce, Lockheed Software Technology Center, emphasized the need for developers to understand who is going to use the software and how it is going to be used, and stated that AI will permit managers and designers to get the job done without conflicting with each other.

Bob Balzer of the Information Sciences Institute outlined the extended automatic programming paradigm. He acknowledged the doubts within the field of software engineering relative to automatic programming by saying, "The notion that formal language specifications will find widespread use is one that makes many of my colleagues roll their eyes." The panelists agreed that AI will continue to play a larger role in software development activities.

RISC inventor and ACM Turing Award recipient John Cocke shown with the 801 minicomputer system built at IBM in the mid-1970s to test RISC technology.

John Cocke receives ACM Turing Award

John Cocke, an IBM fellow at the Thomas J. Watson Research Center and the inventor of reduced instruction set computer (RISC) technology, received the Turing Award October 29 in Dallas. Abraham Peled accepted the award for Cocke, who was ill. The award, presented during the Fall Joint Computer Conference, is ACM's highest honor for technical contributions in computing. It is given annually in commemoration of A.M. Turing, an English mathematician who was a major influence in the early development of computing.

During FJCC, ACM also presented the Distinguished Service Award to Frederick P. Brooks, Jr., the Outstanding Contributions Award to Edward G. Coffman, Jr., the Grace Murray Hopper Award to John K. Osterhout, the President's Award to Kent K. Curtis, and the Software System Award to Adele Goldberg, Daniel H.H. Ingalls, Jr., and Alan C. Kay.

Cocke was cited by the Turing Award Selection Committee for significant contributions to three areas of computer science: RISC development, compiler design and theory, and large-system architecture.

Cocke's other honors include selection last year as a fellow of the American Academy of Arts and Sciences and, in 1985, receipt of the ACM/Computer Society Eckert-Mauchly Award.

Harry Hayman (right), the man for whom the Computer Society named the Harry Hayman Award for Distinguished Staff Service, congratulates True Seaborn, first recipient of the honor.

Computer Society's Seaborn presented first Hayman award as 46 are honored

H. True Seaborn, editor and publisher of the Computer Society and its six magazines, was presented the first Harry Hayman Award for Distinguished Staff Service October 27, during FJCC in Dallas. In addition, the society presented awards to 45 other men and women for the valuable contributions they've made toward its progress.

The highest honor a Computer Society staff member can receive, the Hayman award was established in 1985 to honor the retirement of its distinguished first executive secretary whose career exemplified the highest ideals of society staff service.

The plaque honoring Seaborn recognizes "his many years of excellent, dedicated, and innovative leadership and service" and bears the signatures of the society's president, Roy Russo, and its executive director, T. Michael Elliott. They're key members of the Executive Committee, the unit that voted to honor Seaborn with the first Hayman award.

Seaborn has been a leader in the society's emergence from an organization with 16,000 members in 1973, when he became editor and publisher, to one with more than 90,000 this year.

During his tenure, *Computer* magazine has gained an international reputation for excellence and has experienced a five-fold expansion in circulation, and five new society magazines have been launched. They are *IEEE Computer Graphics & Applications, IEEE Micro, IEEE Design & Test, IEEE Software,* and *IEEE Expert.*

Seaborn has also been a major contributor to many other successful society programs, including numerous professional conferences and initiation of the Computer Society Press.

Following a number of years of volunteer service to the then-Computer Group of the IEEE, Harry Hayman was asked to join the staff as executive secretary on a full-time basis in 1972. He applied the kind of management techniques he learned during his professional career, which included a term as one of the leading computer experts on the US Apollo project, and thus guided the CS through 12 years of growth.

The IEEE developed into the world's largest professional organization during his CS tenure, and the Computer Society evolved as the IEEE's largest unit.

Additional awards. The presentation of eight Distinguished Service Certificates topped the remaining CS honors handed out at FJCC. Recipients of the certificates were

Kenneth R. Anderson of Siemens Research & Technology, for continued and outstanding leadership in technical committee activities and for providing inspiration and guidance in public policy and human resources activities.

James H. Aylor of the University of Virginia, for continued and outstanding leadership and as vice president of conferences and tutorials in 1986-87.

J. Tom Cain of the University of Pittsburgh, for continued and outstanding leadership, for service as vice president of publications in 1986-87, and for serving as acting president of the society during the fourth quarter of 1986.

Ronald G. Hoelzeman of the University of Pittsburgh, for continued and outstanding leadership in publications, financial planning, and educational activities in the society and the computer profession.

Michael C. Mulder of the University of Portland, for continued and outstanding leadership in the quality of the society's educational activities and its *Computer* magazine, and for dedicated service on the Board of Governors in 1986-87.

Dick B. Simmons of Texas A&M University, for continuous and outstanding leadership on intersociety activities.

Joseph Urban of the University of Miami, for outstanding leadership in founding the Technical Committee on Computer Languages and its conference, and for excellence in guiding the society's financial program as treasurer in 1986-87.

Stanley Winkler, for outstanding and continued leadership on intersociety activities, including chairing the first Fall Joint Computer Conference in 1986.

Mary Ellen Curto, Roger Fujii, Sallie V. Sheppard, Bruce D. Shriver, Merlin G. Smith, and Harold S. Stone were presented Outstanding Contributions Certificates.

Meritorious Service Certificates went to Paul L. Borrill, Jon T. Butler, Bill D. Carroll, Ashok K. Chandra, T. Michael Elliott, Gerald L. Engel, Harvey A. Freeman, William R. Habingreither, Lansing Hatfield, Paul L. Hazan, Albert S. Hoagland, Willis K. King, Glen G. Langdon, Duncan H. Lawrie, Ming T. Liu, Amar Mukherjee, John Musa, H. Troy Nagle, Jr., Bernard T. O'Lear, Charles B. Silio, Martha Sloan, Chip G. Stockton, Earl E. Swartzlander, Helen M. Wood, and Marshall C. Yovits.

Barry Boehm, Violet S. Doan, Susan L. Rosenbaum, Sallie V. Sheppard, Wing N. Toy, Gio Wiederhold, and Akihiko Yamada were presented Certificates of Appreciation.

Tokyo Compsac called most successful in conference's history

Toshiro Ohno of Japan Business Automation, Tosiyasu Kunii of Tokyo University, Masanori Ozeki of Japan's Railway Technical Research Institute, and Tadashiro Sekimoto of NEC (left to right) converse at Compsac's opening banquet in Tokyo. Sekimoto thanked the conference organizers and the Computer Society for honoring Japan by holding the conference in the Japanese capital.

For the first time in its 11-year history, the Computer Society's Computer Software and Applications Conference was held outside Chicago. The 11th Compsac took place October 5-9 in Tokyo to acknowledge Japanese contributions to software technology. It will return to Chicago in 1988.

Steve Yau, the honorary conference cochair and a professor at Northwestern University, called Compsac 87 the most successful in the history of the series. At the welcoming banquet, Tadahiro Sekimoto, president of NEC and of the Information Processing Society of Japan, raised a toast to the success of the conference and thanked the Computer Society for honoring Japan by holding Compsac in Tokyo. The IPSJ cosponsored the conference.

The keynote speakers underscored Japan's contributions in markedly different ways. Shizuma Komijima, the vice minister for Japan's Ministry of International Trade and Industry, spoke of Japan's efforts to transform itself into an information society and briefly described the three government-industry cooperative efforts—the Tron everyday-computer project, the ICOT fifth-generation language project, and the Sigma development-environment project—to develop the technologies to accomplish this. MITI is also considering establishing an information university, he said.

Because software-development methods have yet to be transformed by a computing version of the Industrial Revolution, it takes more programmers than available to write the software needed for an information society, Sekimoto said. Japan's goal is to put software-development technology through such a revolution in production techniques, he said.

Japan's growing strength in this technology—a strength helped by long-term government direction and multi-company cooperation—concerns the US, which fears Japan's traditionally closed society may not contribute to worldwide knowledge despite benefitting from the contributions of other nations, said L. Desaix Anderson, the US chargé d'affaires in Tokyo. The flow of information must be equal in both directions, he said. Anderson also complained that Japanese copyright laws were not strong enough to protect US software developers.

Together, the conference and tutorials drew 728 people, more than in recent years. Of the attendees, 683 were on hand exclusively to participate in conference activities; 661 attended from the host nation, and 66 travelled from the US.

Compcon Spring 88 to be broad-based, but will also focus on the specialist

By providing specialized multiple one-day tracks featuring expert speakers, research paper presentations, and panel discussions, Compcon Spring 88 promises to provide a broad-based update of important areas of computer research and development and a focus for the computing specialist as well.

The oldest of the Computer Society's conferences, the event is scheduled March 1-3 in San Francisco, with tutorials the day before and the day after, February 29 and March 4.

The track topics and featured speakers will include "RISC (Reduced Instruction Set Computer) Architectures" by John Hennessy of Stanford University; "Advances in Device Technology," Michael Callahan, AMD; "Computer Augmentation and Workstations," C. Gordon Bell, National Science Foundation; "Neural Networks," Federico Faggin, Synaptics; and "Implications of Superconductivity." The speaker on the final topic has not yet been determined.

Each of the tracks will be initiated in the morning by its featured speaker.

In addition, the neural network track will include three sessions. The opening session will present an "Introduction to Biological Nervous Systems," "Introduction to Neural Models,"and "Introduction to Neural Network Models."

"Implementations of Neural Networks" will be the theme of the second session, which will consist of presentations on software simulations systems, VLSI implementations, and simulations of systems of neural networks.

The third session will feature a panel discussion titled "Perspectives on Neural Networks." It will provide a comprehensive and realistic view of neural nets by panelists ranging from "skeptics to true believers," according to the session chair, Fred Coury. The panelists will have a broad spectrum of interests and will include a neural physiologist, a philosopher, a mathematician, a journalist, and an engineer.

Talks on second-generation LANs stir interest at 12th Local Computer Networks Conference

Discussion of what constitutes second-generation local area networks generated a great deal of interest at the 12th Conference on Local Computer Networks October 5-7 in Minneapolis, Minn.

The two major views expressed were that LANs are either very high performance interconnection hardware composed of 100-megabit fiber optics, or extended network facilities that include network management and qualifiability tools.

As individual LANs grow to include more and more nodes, the performance of the network becomes an important issue. The high-performance fiber optic networks and the network management tools both attempt to provide the necessary performance by either increasing the performance envelope or optimizing network resource utilization.

The growth of individual networks has affected many disciplines, fostering network hierarchical structures, interconnectivity of networks, management and testing of networks, coexistence of networks and nodes, and a growing number of gateway, bridge, and routing products.

A panel session entitled "Second Generation LAN Issues" was devoted to trends toward hierarchically structured networks with very high performance fiber optic "backbones" to which either Ethernet or token-ring type networks are connected. An important supporting device for these hierarchical connections is the gateway or protocol converter. Although the gateway is an important device, the current market is providing more products of network router and bridge type, which connect networks of the same type and protocol. The session was chaired by Harvey Freeman of Lanworks, the conference's standing committee chair.

In a pragmatic panel session, "How to Really Wire Your Building," the issues and problems of design and installation were addressed from the viewpoint of both the product user and the supplier. It seems that, even in new construction, twisted-pair wiring is often used instead of potentially higher performance optical fiber or coaxial cable. There appears to be some hesitancy among building architects to design and specify the newer optical fiber technology over twisted pair, which they have used extensively for other functions such as telephone systems.

The keynote address, entitled "Digital's Strategic Network Vision" and delivered by Robert Murray of Digital Equipment Corporation, indicated that DEC's strong position in the network area is based on the ability to interconnect a wide range of computer systems. DEC has 15,000 Ethernet and 100,000 Decnet installations and expects these numbers to double by next year.

Parallel architectures and algorithms were the focus at CAPAMI 87

New parallel architectures and parallel algorithms for problems in computer vision, image processing, and related areas of artificial intelligence were the prime topics of interest at the Computer Architecture for Pattern Analysis and Machine Intelligence Workshop (CAPAMI 87) in Seattle October 5-7.

Three invited speakers presented their perspectives on current work and new directions for the field.

Masa Kidode of Toshiba reported on image processing architecture research and development in Japan. Up-to-date surveys of Japanese research and development in this field are uncommon. Participants got a glimpse of several new systems from Japan, including a programmable-window-based multiprocessor for visual analysis, a 256 × 256 parallel-cellular array processor, and several personal-computer-based systems.

George Reeke of the Neurosciences Institute at Rockefeller University described his work with Gerald Edelman on neural networks for recognition, categorization, generalization, and visual tracking. This work emphasized the perspective of building computational models that integrate multiple networks responding to various environmental stimuli and maintain spatiotemporal continuity by feedback from interactions of the system with the environment.

Tom Knight of MIT and Symbolics gave his perspective on trends in architectures for vision and AI.

The technical program included 27 refereed papers that comprise the 227-page proceedings, available through the Computer Society Press.

CALL

IEEE Expert is seeking materials for publication. Submit articles on technology and AI applications to David Pessel, Editor-in-Chief, BP America, 4440 Warrensville Center Rd., Cleveland, OH 44128; reports on conferences, short subjects and papers on PCs, products, and resources to Henry Ayling, Managing Editor, *IEEE Expert,* 10662 Los Vaqueros Cir., Los Alamitos, CA 90720; and book reviews to K.S. Shankar, Associate Editor, Federal Systems Division, IBM Corp., 3700 Bay Area Blvd., Houston, TX 77058.

Technical Committee on Computer Education, Computer Society of the IEEE: Contributions are welcomed for the TCCE newsletter, a forum for the exchange of ideas among persons interested in computer education or computers in education. News items, short articles, and correspondence should be sent to Helen Hays, Dept. of Computer Science, Southeast Missouri State University, Cape Girardeau, MO 63701; (314) 651-2244.

Commercial News USA, published by the US Commerce Dept., will promote technology, services, and products related to architecture, engineering, and construction systems in its February 1988 issue. To submit materials, contact Sally Forden, US and Foreign Commercial Service, Rm. 2108, 14th & Constitution Ave. NW, Washington, DC 20230; (202) 377-5367.

CAE India 88, India Computer Graphics International Conference & Exhibition: March 22-25, 1988, New Delhi, India. Submit abstract by **December 16, 1987,** to Tara S. Ganguli, Technology and Research Associates, 5 Lindsay St., Calcutta—700087, India; phone (033) 29-9420.

Third International IEEE Conference on Ada Applications and Environments: May 23-26, 1988, Manchester, N.H. Submit paper by **Dec. 30, 1987,** to Dewayne E. Perry, AT&T Bell Laboratories, Rm. 3D-454, 600 Mountain Ave., Murray Hill, NJ 07974; (201) 582-2529.

Eurographics 88, Ninth Conference of the European Assoc. for Computer Graphics (INRIA): Sept. 12-16, 1988, Nice, France. Submit paper by **Dec. 31, 1987** to INRIA, Service des Relations Exterieures, Domaine de Voluceau—BP 105, 78153 Le Chesnay Cedex, France; telephone (33) 1-39-63-55-01.

15th IFAC Workshop on Real-Time Programming: May 25-27, 1988, Valencia, Spain. Submit draft by **Jan. 1, 1988,** to WRTP 88, Grupo de Informatica Industrial—DSIC/DISCA, Universidad Politecnica de Valencia, PO 22012, E-46071 Valencia, Spain; phone (34) 6-3604041.

OR PAPERS

Call for referees for *Computer*

Referees are sought for special issues of *Computer* that will cover the following topics:

- laser communication technology and systems
- computer-integrated manufacturing
- national computer policies—the computer industry in an international context
- innovative printer technology
- storage technology
- concurrent systems: the hardware, production, maintenance, and software issues
- emerging technologies for computer component, hardware, and software design and production
- high-performance CAD/CAM, engineering/scientific, and programming workstations
- computers in automobiles
- computers in the entertainment and advertising industries
- real-time systems
- Videotext—has the vision failed?

Persons interested in serving as referees are asked to circle Reader Service Number 195 on the Reader Service Card at the back of this magazine and to send the card to the Reader Service Inquiries Dept.

26th Assoc. for Computational Linguistics Meeting: June 7-10, 1988, Buffalo, N.Y. Submit extended draft by **Jan. 4, 1988** to Jerry R. Hobbs, Artificial Intelligence Center, SRI International, 333 Ravenswood Ave., Menlo Park, CA 94025; (415) 859-2229.

Second Symposium on Space C^3 (AFCEA): May 16-19, 1988, Annapolis, Md. Submit abstract by **Jan. 9, 1988,** and final paper by **April 11, 1988,** to Randy Crawford/DQ, IIT Research Institute, 185 Admiral Cochrane Dr., Annapolis, MD 21401; (301) 224-2295.

Avignon 88, 8th International Workshop on Expert Systems & Their Applications (ECCAI): May 30-June 3, 1988, Avignon, France. Submit papers by **Jan. 11, 1988,** to Jean-Claude Rault, EC2, 269-287, rue de la Garenne, 92000 Nanterre, France; phone (33) 1-47-80-70-00.

Fifth International Conference on Testing Computer Software (DPMA): June 13-16, 1988, Washington, DC. Submit extended abstract by **Jan. 14, 1988,** and final paper by **April 1, 1988,** to US Professional Development Institute, 1734 Elton Rd., Suite 221, Silver Spring, MD 20903; (301) 445-4400.

First International Conference on Industrial & Engineering Applications of Artificial Intelligence and Expert Systems: June 2-3, 1988, Tullahoma, Tenn. Submit abstract by **Jan. 15, 1988,** and final paper by **March 31, 1988,** to Moonis Ali, University of Tennessee Space Institute, Tullahoma, TN 37388.

CAD/CAM Technology Transfer to Latin America Conference (IFIP): Aug. 22-26, 1988, Mexico City. Submit paper and abstract on any area of CAD/CAM/CAE by **Jan. 15, 1988** to G. Leon Lastra, Instituto de Investigaciones Electricas, Apdo. Postal 5-849, 11590 Mexico, D.F.

Eighth International Symposium on Protocol Specification, Testing, and Verification (IFIP): June 7-10, 1988, Atlantic City, N.J. Submit paper by **Jan. 15, 1988** to Sudhir Aggarwal, Bell Communications Research, 435 South St., Morristown, NJ 07960; (201) 829-4477; or Krishan Sabnani, AT&T Bell Laboratories, 600 Mountain Ave., Murray Hill, NJ 07974; (201) 582-5740.

17th International Conference on Parallel Processing: Aug. 15-19, 1988, St. Charles, Ill. Complete manuscripts (for regular papers) or summaries (for short papers) are sought by **Jan. 15, 1988.** Submit papers on algorithms and applications to David H. Bailey, Mail Stop 258-5, NASA Ames Research Center, Moffett Field, CA 94035; on software to Howard E. Sturgis, Xerox Corp., Palo Alto Research Center, 3333 Coyote Hill Rd., Palo Alto, CA 94304; and on hardware and other areas to Faýe A. Briggs, Sun Microsystems, Inc., 2550 Garcia Ave., Mountain View, CA 94043.

Third International Conference on Applications of Artificial Intelligence in Engineering: Aug. 8-12, 1988, Stanford, Calif. Submit paper by **Jan. 15, 1988,** to John Gero, Dept. of Architectural Science, University of Sydney, NSW 2006 Australia; phone (61) 2-692-2328; and R. Adey, Computational Mechanics Institute, 25 Bridge St., Billerica, MA 01821; (617) 667-7582.

Workshop & Symposium on Formal Techniques in Real-time and Fault-tolerant Systems: Sept. 20-23, 1988, Coventry, England. Submit papers and extended extracts by **Jan. 15, 1988,** to M. Joseph, Dept. of Computer Science, University of Warwick, Coventry, CV4 7AL, UK.

19th Pittsburgh Conference on Modeling and Simulation (IEEE, ISA, SCS): May 5-6, 1988, Pittsburgh. Submit summary and abstract by **Jan. 31, 1988,** and final manuscript by **May 6, 1988,** to William G. Vogt or Marlin H. Mickle, Modeling and Simulation Conference, 348 Benedum Engineering Hall, University of Pittsburgh, Pittsburgh, PA 15261.

Eurocrypt 88, Workshop on the Theory and Application of Cryptologic Techniques (IACR): May 25-27, 1988, Davos, Switzerland. Submit abstract by **Jan. 31, 1988,** to Ingemar Ingemarsson, Dept. of Electrical Engineering, Linkoping University, S-581 83 Linkoping, Sweden.

IEEE Software: Submit articles on any topic for the September 1988 issue by **Feb. 1, 1988,** to Ted G. Lewis, Editor-in-Chief, *IEEE Software,* c/o Computer Science Dept., Oregon State University, Corvallis, OR 97331; (503) 754-2744; CSnet lewis@oregon-state; Compmail+ t.lewis.

IEEE Software* and *IEEE Expert: Papers are sought for special November 1988 issues on expert systems applied to software engineering. Submit abstract as soon as possible and eight copies of manuscript by **Feb. 1, 1988,** to Murat Tanik, Dept. of Computer Science & Engineering, Southern Methodist University, Dallas, TX 75275-0122; (214) 692-3083, ext. 2854.

Conferences that the Computer Society sponsors or participates in are indicated by the Computer Society logo; additional conference sponsors are listed in parentheses. Other conferences of interest to our readers are also included.

For inclusion in Call for Papers or Calendar, submit information **six weeks before the month of publication** (e.g., for the **February 1988** issue, send information for receipt by **Dec. 15, 1987**) to Calendar Editor, *Computer,* 10662 Los Vaqueros Cir., Los Alamitos,CA 90720.

CALENDAR

December 1987

Winter Simulation Conference, Dec. 14-16, Atlanta. Contact Hank Grant, Factrol, Inc., PO 2569, West Lafayette, IN 47906; (317) 463-3637.

Eighth International Conference on Computing Methods in Applied Sciences and Engineering (INRIA), Dec. 14-18, Versailles, France. Contact INRIA, Service des Relations Exterieures, Bureau des Colloques, Domaine de Voluceau, Rocquencourt, BP 105, 78153 Le Chesnay Cedex, France; phone 33 (1) 39-63-56-00.

January 1988

HICSS 88, 21st Hawaii International Conference on System Sciences, Jan. 5-8, Kailua-Kona, Hawaii. Contact Ralph H. Sprague, Jr., Decision Sciences Dept., University of Hawaii, 2404 Maile Way, E-303, Honolulu, HI 96822; (808) 948-7430.

23rd Computer Society of India Convention, Jan. 6-9, Madras, India. Contact Convention Office, CSI HQ Bldg., CPT Campus, Taramani, Madras 600 113.

Simulation in Engineering Education Conference, Jan. 7-8, San Diego. Contact Society for Computer Simulation, PO 17900, San Diego, CA 92117; (619) 277-3888.

Third Technical Symposium on Optoelectronics and Laser Applications in Science and Engineering (SPIE), Jan. 10-15, Los Angeles. Contact Jane Lybecker, SPIE, PO 10, Bellingham, WA 98227; (206) 676-3290.

Annual IEEE Design Automation Workshop, Jan. 13-15, Apache Junction, Ariz. Contact Walling Cyre, Control Data, HQM 173, Box 1249, Minneapolis, MN 55440; (612) 853-2692.

15th SIGAct, SIGPlan Symposium on Principles of Programming Languages (ACM), Jan. 13-15, San Diego. Contact Jeanne Ferrante, IBM Hawthorne H2-B54, Box 218, Yorktown Heights, NY 10598; (914) 789-7529.

Third Conference on Hypercube Concurrent Computers and Applications, Jan. 19-20, Pasadena, Calif. Contact Patricia McLane, Jet Propulsion Laboratory, MS 180-205, Pasadena, CA 91109; (818) 354-5556.

Workshop on High-Level Synthesis (ACM), Jan. 24-27, Orcas Island, Wash. Contact Ewald Detjens, Exemplar Logic, 1820 Carleton St., Berkeley, CA 94703; (415) 849-2020.

International Workshop on Software Version and Configuration Control (GI), Jan. 27-29, Grassau, West Germany. Contact Peter Feiler, SEI, Carnegie Mellon University, Pittsburgh, PA 15213; (412) 268-7790.

February 1988

Cairo International Computer Conference (IASTED), Feb. 1-3, Cairo. Contact Secretariat, PO 354, CH-8053, Zurich, Switzerland.

Fourth International Conference on Data Engineering, Feb. 1-5, Los Angeles. Contact Benjamin W. Wah, Dept. of Electrical and Computer Engineering, University of Illinois, Urbana, IL 61801; (217) 333-3516.

Multiconference 88 (SCS), Feb. 3-5, San Diego. Contact Society for Computer Simulation, PO 17900, San Diego, CA 92117; (619) 277-3888.

Second Conference on Applied Natural Language Processing (ACL), Feb. 9-12, Austin, Texas. Contact Donald Walker, Bell Communications Research, 445 South St., MRE 2A379, Morristown, NJ 07960; (201) 829-4312.

Winter Unix Technical Conference, Feb. 9-12, Dallas. Contact Usenix Assoc. Conference Office, PO 385, Sunset Beach, CA 90742; (213) 592-1381.

Sixth International Symposium on Applied Informatics (IASTED), Feb. 16-18, Grindelwald, Switzerland. Contact IASTED, PO 354, CH-8053, Zurich, Switzerland.

16th ACM Computer Science Conference, Feb. 23-25, Atlanta. Contact ACM, 11 W. 42nd St., New York, NY 10036.

CSC 88, 16th Annual Computer Science Conference (ACM), Feb. 23-25, Atlanta. Contact Lucio Chiaraviglio, School of Information and Computer Science, Georgia Institute of Technology, Atlanta, GA 30332; (404) 894-3152.

Vision Guidance for Robotic Systems (SME), Feb. 23-25, Cincinnati. Contact Joanne Rogers, Society of Manufacturing Engineers, 1 SME Dr., Dearborn, MI 48121; (313) 271-1500.

SIGCSE Symposium (ACM), Feb. 25-26, Atlanta. Contact ACM, 11 W. 42nd St., New York, NY 10036.

NOMS 88, IEEE 1988 Network Operations and Management Symposium, Feb. 28-March 2 New Orleans. Contact IEEE Communications Society, 345 E. 47th St., New York, NY 10017; (212) 705-7857.

10th National Computer Conference (IEEE), Feb. 28-March 2, Jeddah, Saudi Arabia. Contact Athar Javaid, IEEE, PO 8900, Jeddah 21492, Saudi Arabia.

Symposium on Information Systems as a Resource to Support Managerial Decision-Making, Feb. 29-March 3, Sydney, Australia. Contact IFIP, 3 rue de Marche, CH-1204, Geneva, Switzerland.

Compcon Spring 88, Feb. 29-March 4, San Francisco. Contact Hasan al-Khatib, Dept. of Electrical Engineering and Computer Science, Santa Clara University, Santa Clara, CA 95053; (408) 554-4485.

March 1988

Ninth Conference on EDP Performance and Capacity Management, March 7-8, Scottsdale, Ariz. Contact Applied Computer Research, PO 9280, Phoenix, AZ; (602) 995-5929.

Second International Conference on Computer Workstations, March 7-10, Santa Clara, Calif. Contact Patrick Mantey, 335A Applied Science Bldg., Dept. of Computer Engineering, University of California at Santa Cruz, Santa Cruz, CA 95064; (408) 429-2158.

Federal Office Systems Expo, March 7-10, Washington, DC. Contact NTP, 2111 Eisenhower Ave., Suite 400, Alexandria, VA 22314; (703) 683-8500.

Southcon 88 (IEEE, ERA), March 8-10, Orlando, Fla. Contact Southcon 88, 8110 Airport Blvd., Los Angeles, CA 90045; (213) 772-2965.

1988 International Zurich Seminar on Digital Communications, March 8-11, Zurich. Contact Secretariat IZS 88, c/o P. Gunzburger, Hasler AG, TDS, Belpstrasse 23, CH-3000 Bern 14, Switzerland; phone 41 (31) 63-28-08.

1988 International Development Center Conference (DCI), March 13-16, Orlando, Fla. Contact Development Center Institute, PO 44087, Indianapolis, IN, 46244-0087; (317) 846-2753.

Sixth National Conference on Ada Technology, March 14-17, Washington, DC. Contact Al Rodriguez, US Army Communications-Electronics Command, AMSEL-

RD-LC-ASST-1A, Fort Monmouth, NJ 07703; (201) 532-4725.

Fourth International Conference on Artificial Intelligence Applications, March 14-18, San Diego. Contact AI Conference, Computer Society, 1730 Massachusetts Ave., NW, Washington, DC 20036-1903; (202) 371-1013.

International Conference Extending Data Base Technology (AICA, GI, AFCET, BCS), March 14-18, Venice, Italy. Contact Joachim W. Schmidt, Universitat Frankfurt, Fachbereich Informatik, Dantestrasse 9, D 6000 Frankfurt 1, West Germany; phone (49) 69-7988101.

Securicom 88, Sixth Worldwide Congress on Computer and Communications Security and Protection, March 15-17, Paris. Contact Securicom 88, 8, rue de la Michodiere, 75002 Paris, France; phone (33) 1-47-42-41-00.

Seventh IEEE Phoenix Conference on Computers and Communications, March 16-18, Scottsdale, Ariz. Contact Carl Ryan, Motorola GEG, 2501 S. Price Rd., Chandler, AZ 85248-2899; (602) 732-3074.

21st Simulation Symposium (SCS, IMACS), March 16-18, Tampa, Fla. Contact Alfred Jones, Computer Science Dept., Florida Atlantic University, Boca Raton, FL 33431; (305) 393-3675.

Western Educational Computing Workshops (CECC), March 17-18, Norwalk, Calif. Contact Alexia Devlin, San Francisco State University, Accounting Data, NADM-358, 1600 Holloway Ave., San Francisco, CA 94132.

NCGA 88, Ninth Conference and Exposition Dedicated to Computer Graphics Applications, March 20-24, Anaheim, Calif. Contact NCGA 88, National Computer Graphics Assoc., 2722 Merrilee Dr., Suite 200, Fairfax, VA 22031.

Compstan 88, Computer Standards Conference, March 21-23, Arlington, Va. Contact James Hall, US Dept. of Commerce, National Bureau of Standards, Technology Bldg. 225, Rm. B266, Gaithersburg, MD 20899; (301) 975-3273.

RIAO 88, User-Oriented Content-Based Text and Image Handling Conference (AFIPS), March 21-24, Cambridge, Mass. Contact RIAO 88, Conference Service Office, Massachusetts Institute of Technology, Bldg. 7, Rm. 111, Cambridge, MA 02139; or CID, 36 bis rue Ballu, 75009 Paris, France.

Sixth IEEE VLSI Test Workshop, March 22-23, Atlantic City, N.J. Contact Wesley E. Radcliffe, IBM East Fishkill, Dept. 277, Bldg. 321-5E1, Hopewell Junction, NY 12533; (914) 894-4346.

AAAI Spring Symposium, March 22-24, Palo Alto, Calif. Contact American Assoc. for Artificial Intelligence, 445 Burgess Dr., Menlo Park, CA 94025-3496; (415) 328-3123.

CAE India 88, India Computer Graphics International Conference & Exhibition, March 22-25, New Delhi, India. Contact Tara S. Ganguli, Technology and Research Associates, 5 Lindsay St., Calcutta—700087, India; phone (033) 29-9420.

COIS 88, Conference on Office Information Systems (ACM), March 23-25, Palo Alto, Calif. Contact Robert Allen, 2A-367, Bell Communications Research, Morristown, NJ 07960; (201) 829-4315.

Extending Database Technology (IASI, INRIA), March 23-25, Venice, Italy. Contact Stefano Ceri, Politecnico di Milano, Dipart. di Elektronika, Piazza Leonardo da Vinci 32, 20133 Milano, Italy; phone 39 (02) 23-67-241.

Fourth International Conference on Pattern Recognition (BPRA, IAPR), March 28-30, Cambridge, England. Contact J. Kittler, Dept. of Electronic and Electrical Engineering, University of Surrey, Guildford GU2 5XH, England, UK.

Infocom 88, March 28-31, New Orleans. Contact Infocom 88, Computer Society of the IEEE, 1730 Massachusetts Ave. NW, Washington, DC 20036-1903; (202) 371-1013.

April 1988

Conference on the Human Dimension in Artificial Intelligence, April 6-9, Lexington, Ky. Contact Engineering Continuing Education, 223 Transportation Research Bldg., University of Kentucky, Lexington, KY 40506-0043; (606) 257-4295.

International Workshop on Robot Control: Theory and Applications (IEE), April 11-12, Oxford, England. Contact the Computing and Control Division, IEE, Savoy Pl., London WC2R 0BL; phone 44 (01) 240-1871, ext. 330.

Computer Networking Symposium, April 11-13, Washington, DC. Contact George K. Chang, Bell Communications and Research, 6 Colbert Pl., Piscataway, NJ 08854; (201) 699-3879.

CompEuro 88, April 11-15, Brussels. Contact Jacques Tiberghien, VRIJE Universiteit Brussels, Pleinlaan 2, 1050 Brussels, Belgium; phone 32 (02) 641-29-05.

ICSE 88, 10th International Conference on Software Engineering (ACM), April 11-15, Raffles City, Singapore. Contact Tan Chin Nam or Lim Swee Say, 71 Science Park, Singapore 0511; phone (65) 772-0200.

IPC 88, 17th International Programmable Controllers Conference (ESD, SMI), April 12-14, Detroit. Contact IPC 88, 100 Farnsworth, Detroit, MI 48202; (800) 457-9504.

Manufacturing International 88 (ASME), April 17-20, Atlanta. Contact Meetings Dept., American Society of Mechanical Engineers, 345 E. 47th St., New York, NY 10017; (212) 705-7788.

1988 IEEE Symposium on Security and Privacy, April 18-21, Oakland, Calif. Contact Dave Bailey, US Dept. of Energy, Production Operations Division/CIM Office, PO 5400, Albuquerque, NM 87115; (505) 846-4600.

Eastern Simulation Conference (SCS), April 18-21, Orlando, Fla. Contact Society for Computer Simulation, PO 17900, San Diego, CA 92117; (619) 277-3888.

11th IEEE Workshop on Design for Testability, April 19-22, Vail, Colo. Contact T.W. Williams, IBM Corp., PO 1900, Dept. 67A/021, Boulder, CO 80301-9191; (303) 924-7692.

International Conference on Electronic Publishing, Document Manipulation, and Typography (INRIA), April 20-22, Nice, France. Contact INRIA, Service des Relations Exterieures, Bureau des Colloques, Domaine de Voluceau, Rocquencourt—BP 105, F-78153 Le Chesnay Cedex, France.

Second International Conference on Expert Database Systems, April 25-28, Tysons Corner, Va. Contact Edgar H. Sibley, George Mason University, ICSE Dept., 4400 University Dr., Fairfax, VA 22030.

IEEE International Conference on Robotics and Automation, April 25-29, Philadelphia. Contact Harry Hayman, 738 Whitaker Terrace, Silver Spring, MD 20901; (301) 434-1990.

Sococo 88, Symposium on Software for Computer Control (IFAC, IFIP), April 26-28, Johannesburg, South Africa. Contact IFIP, 3 rue de Marche, CH-1204, Geneva, Switzerland.

Second Expert Systems Conference (ESD, SMI), April 26-28,, Dearborn, Mich. Contact Engineering Society of Detroit, 100 Farnsworth, Detroit, MI 48202; (800) 457-9504.

May 1988

Artificial Intelligence and Advanced Computer Technology Conference and Exhibition (SCS), May 4-6, Long Beach, Calif. Contact Tower Conference Management Co., 331 W. Wesley St., Wheaton, IL 60187; (312) 668-8100.

19th Pittsburgh Conference on Modeling and Simulation (IEEE, ISA, SCS), May 5-6, Pittsburgh. Contact William G. Vogt or Marlin H. Mickle, Modeling and Simulation Conference, 348 Benedum Engineering Hall, University of Pittsburgh, Pittsburgh, PA 15261.

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- ☐ Society of Aircraft Materials and Processes (SAMPE)
- ☐ Society of Automotive Engineers (SAE)
- ☐ Society for Industrial and Applied Mathematics (SIAM)
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UNIVERSITY OF PITTSBURGH
DEPARTMENT OF COMPUTER SCIENCE
Junior and Senior Faculty Positions

The Department of Computer Science has entered a period of substantial growth. At least five tenure track faculty positions are to be filled as soon as possible, before the end of 1988. Responsibilities include research, supervision of graduate student research and graduate and undergraduate teaching. A Ph.D. in computer science or in a closely related field is required. Any area of specialty in computer science will be considered, although preference will be given to programming languages, software engineering, database systems, algorithms, theoretical computer science, artificial intelligence and telecommunications. Salary and rank will be commensurate with a candidate's established record of scholarly achievement and/or research potential.

The Department has nineteen full-time faculty members, strong graduate (M.S. and Ph.D.) and undergraduate (B.S.) programs. It has an excellent research library. Departmental computing facilities include a VAX 11/780 (under bsd UNIX), a PDP 11/70 (UNIX), several smaller PDP-11 systems, a variety of microcomputers, several graphics systems, fourteen SUN workstations, and a network of Xerox 1100-series (Dandelion) workstations. The research systems are accessible via the Department's Ethernet-compatible LAN. Convenient access is also provided to the extensive general computer facilities of the University as well as to other networks (e.g. CSNET). The Department operates the Research Institute for Parallel and Distributed Intelligence Systems (IPDIS) to provide an environment for innovative research in computer science, and cooperates closely with the Pittsburgh Supercomputing Center.

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Please send your resume to: Dr. Shi-Kuo Chang, Chair, Department of Computer Science, University of Pittsburgh, Pittsburgh, PA 15260. CSNet Address: CHANG@PITT.

UNIVERSITY OF CALIFORNIA AT DAVIS

The Computer Science Division of the University of California at Davis invites applications from highly qualified individuals for several tenure-track positions. The Division is especially interested in senior candidates with research strengths in the fields of computer architecture, networks, and VLSI design. Outstanding candidates in other fields will also be considered. Rank and salary will be commensurate with qualifications. In addition to teaching competence, applicants must have a distinguished research record.

The Division of Computer Science is an independent unit within the Department of Electrical Engineering and Computer Science. Its interests cover the mainstream areas of computer science, including artificial intelligence, computer architecture, computer systems design, database systems, computer graphics, computer security, fault tolerant computers, networking, numerical analysis, program specification and verification, operating systems, performance evaluation, robotics, software engineering and theoretical computer science. Current research strengths and facilities exist in the areas of computer graphics, theory, computer systems research, image processing, and robotics.

The Division is in a period of building and growth, with the aim of becoming one of the leading computer science departments in the nation. The department administers undergraduate majors in Computer Science Engineering, Computer Science and Mathematics, and it has an active MS/PhD program with a heavy emphasis on research. Its expanding departmental research facilities include an Encore Multimax processor, several VAX systems (8600, 785, etc.), two Iris graphics workstations, a Ridge 32, numerous Sun, Microvax II and Apollo work stations, and a number of special purpose systems all linked through Ethernet and serial communications networks. Other LAN systems are available, for instruction and research. General purpose campus facilities are available, and the supercomputer resources of the Lawrence Livermore National Laboratories are also accessible.

UC Davis is the third largest of the University of California campuses. It shares with the other campuses of the UC system a strong commitment to leadership in education and research. Davis is close to the major areas of computer science and electronics activity in northern California and thus is in a strategic position to play a key role in future developments of the discipline.

The town of Davis has a population of approximately 50,000. Located eleven miles from Sacramento, it is situated within driving distance from the major cultural centers of the San Francisco area as well as the outstanding recreational facilities of the Sierra Nevada. The town has earned an international reputation for its progressive energy-conservation policies. Because of its location, its climate, and its sophisticated small town character, Davis is considered by many to be an ideal living environment.

Interested applicants should send a curriculum vitae with the names of at least three professional references to Richard F. Walters, Chair, Division of Computer Science, or to S. Louis Hakimi, Chair, Department of Electrical Engineering and Computer Science, University of California, Davis, CA 95616.

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THE OHIO STATE UNIVERSITY
Department of Computer and Information Science

Applications are invited for faculty positions at all levels. A Ph.D. in computer science or a closely related field is required. Of special interest are candidates in the areas of artificial intelligence, computer graphics, databases, numerical analysis, programming languages, operating systems, parallel and distributed computing, software engineering, and VLSI design. Special research support packages are available for highly qualified candidates.

Computing facilities within the Department include a DEC-2060, three Pyramids, 20 Sun-3 workstations, 10 IBM RTs, 15 Xerox LISP machines, an Intel iPSC/5 Hypercube, an Encore Multimax, a BBN Butterfly, numerous other systems for graphics, robotics, etc., and over 300 Macintoshes. Macs are used in introductory computing courses. An additional 200 Sun-3 workstations and 6 Hewlett Packard color graphics workstations will be installed this year for other instructional use. The OSU Computing Center facilities include a Cray XMP, IBM 3081-D, and several IBM 4341s. All systems are attached to a campus-wide fiber optic network (Pronet 80) using TCP/IP protocols. Access is available to the national networks (ARPANET, CSNET, BITNET, USENET).

To apply, please send application and resume to Prof. Ming T. (Mike) Liu, Chairman of Faculty Search Committee, Department of Computer and Information Science, The Ohio State University, 2036 Neil Avenue, Columbus, Ohio 43210-1277 Ohio-State.) In order to expedite consideration, please ask three references to send their confidential letters directly to Prof. Liu. The Ohio State University is an equal opportunity/affirmative action employer.

GEORGE WASHINGTON UNIVERSITY
TENURE-TRACK
FACULTY POSITIONS

The Department of Electrical Engineering and Computer Science invites applications for tenure-track faculty positions in Electrical Engineering and Computer Science. Candidates should have an earned doctorate and research experience, with an interest in both teaching and research. Ability to attract research grants and contracts for support of faculty and student assistants is valued. The George Washington University is located in the center of Washington, DC. This metropolitan area sustains the second largest concentration of research and development activity in the United States which creates a continuing demand for rigorously trained engineers as well as broad research opportunities. Our department is the largest department in the School of Engineering and Applied Sciences with 37 full-time faculty, and a large graduate and undergraduate student body. The department has an annual research budget of close to $1 million. Send Curriculum Vita, list of publications and references, to:

Professor Roger H. Lang, Chairman
Department of Electrical Engineering and Computer Science
School of Engineering & Applied Sciences
THE GEORGE WASHINGTON UNIVERSITY
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WRIGHT STATE UNIVERSITY
Computer Science & Engineering

Applicants are invited for full-time positions in Computer Science and/or Computer Engineering at all faculty levels. There is particular interest in professors who have sufficient experience, currency, and depth to direct doctoral students and research dissertations in a PhD program in Computer Science & Engineering. The Department is also interested in PhD's with less experience, but who have a commitment to research and teaching in a PhD granting program. Rank and competitive salaries are determined by qualifications and experience.

The State supported university is located in a high technology environment among industrial/military research and development facilities. An associated State assisted research park fostering basic and applied industrial/military/university research is active and growing impressively. The University has identified computer science & computer engineering as an area of high priority for continued development.

Department strenghts include a large faculty, extensive laboratory facilities, research programs, industrial/military support, degree programs in both computer science and computer engineering, and large student populations at graduate as well as undergraduate levels.

Successful candidates for tenure-track positions should have a Ph.D in Computer Science, Computer Engineering, or equivalent background, and have demonstrated a strong research, as well as teaching, commitment. Any non-tenure-track positions will be filled by candidates with strong computer science or computer engineering credentials. At least a Master of Science Degree in the field is desired.

Please submit detailed resumes including names of 3 references to: Professor Larry A. Crum, Chair, Department of Computer Science, Wright State University, Dayton, Ohio 45435. Reviewing for tenure-track positions will begin October 1, 1987 and for non-tenure-track positions on March 1, 1988. Reviewing will continue monthly until positions are filled or until September 1, 1988.

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UNIVERSITY OF MARYLAND
Institute for Advanced Computer Studies

The University of Maryland Institute for Advanced Computer Studies (UMIACS) was established in 1985 as an independent state-funded research unit. UMIACS, while residing on the College Park campus, is intended to serve the entire University of Maryland system as a focal point for research activities in computing.

UMIACS has 25 tenure track research faculty lines, in addition to a substantial operating budget to support the research activities of its faculty. Most faculty members in UMIACS will hold joint appointments with academic departments on the campus; their teaching responsibilities would be reduced according to their percentage appointments in UMIACS.

Several faculty positions have been reserved for permanent, full-time appointments in the Institute. These appointments are for senior level faculty and will include commitments from the Institute for research support (e.g. equipment, travel, graduate students, etc.) Applicants for these permanent positions should send a complete resume and names of four references to Prof. Larry S. Davis, Director, University of Maryland Institute for Advanced Computer Studies, College Park, MD 20742. The University of Maryland is an equal opportunity and affirmative action employer. Women and minorities are encouraged to apply.

CLARKSON UNIVERSITY
Department of Electrical and Computer Engineering

Applications are invited for the position of Chairperson, which will become available on July 1, 1988. The requirements include: an earned PhD degree in electrical engineering or a closely related discipline; distinguished accomplishments in both engineering education and research; and an ability to provide dynamic leadership. The position requires academic administration of the department, while continuing to maintain interaction with the students in the form of teaching and research. There are currently 25 full time faculty members, 800 undergraduates, and 60 graduate students working toward MS and PhD degrees. The research areas are diverse and include communications, computer engineering, control and robotics, electromagnetics, power engineering, and solid state. Annual grants and contracts total approximately $1M. The chairperson should provide the driving force in an ongoing effort to improve the strengths of the department, in terms of both quality funded reserach and excellence in teaching. Clarkson is a small independent college specializing in engineering, science, and management. The total student population is approximately 4000, of which 10% are studying at the graduate level. Clarkson is situtated in Northern New York, lying between the St. Lawrence River and the Adirondak mountains. Neighboring colleges include St. Lawrence University and Potsdam College. Please send a resume and 3 references, by February 29, 1988, to Dr. Paul B. McGrath, Department of Electrical and Computer Engineering, Clarkson University, Potsdam, NY 13676. Clarkson is an Equal Opportunity/Affirmative Action employer. MFVH

UNIVERSITY OF CALIFORNIA, DAVIS
Faculty Positions in Electrical Engineering and Computer Science

The Department of Electrical Engineering and Computer Science at UC Davis invites applications for tenure track positions at all ranks. The primary areas of interest are image processing, computer engineering, and computer science.

The department, with forty-six faculty members and 150 full-time graduate students, is experiencing rapid growth. Our College is the nation's sixteenth largest producer of engineering Ph.D.'s in a University which has the nineteenth largest extramural research funding. Salary and benefits are extremely attractive.

Davis is a pleasant, family-oriented community near Sacramento, within easy driving distance to Silicon Valley, the Lawrence Livermore National Laboratory, San Francisco, the Pacific Ocean, and the Sierra Nevada Mountains.

We are seeking individuals with strong records of teaching and research with ambitious plans. Senior appointments require outstanding records of achievement; junior appointments must show evidence of great promise. All faculty are expected to have a strong commitment to teaching at all degree levels, and to demonstrate the ability to attract significant research support.

The positions require a Ph.D. degree or equivalent, and are open until filled. Send a resume and the names of at least three references to:

Professor S. Louis Hakimi, Chair
Department of Electrical Engineering and Computer Science
University of California
Davis, CA 95616

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UNIVERSITY OF CALIFORNIA, SANTA CRUZ
Computer Engineering
Computer and Information Sciences

The CE and CIS Boards of Studies invite applications, as appropriate, for tenure track positions as Assistant, Associate or Full Professor, effective July 1, 1988. UCSC is the University of California campus nearest to "Silicon Valley" where it is developing close research ties with local industry in the computer field. Faculty salaries are competitive, and opportunities for consulting are extensive.

Computer Engineering has openings, tenured or untenured as appropriate, with emphasis given to faculty with research focus in software engineering; computer architecture, compiler construction, communications; and parallel environments (#63-867); or special purpose architectures, VLSI, graphics; signal and image processing, and computer architecture (#31-856).

A Ph.D. in Computer Engineering, Electrical Engineering, Computer Sciences or equivalent, and a solid research record as evidenced by publication in technical journals is required. Applicants will be evaluated on their research record, teaching, professional activities and demonstrated (or potential) leadership in their field. Industrial experience will be favorably considered. Candidates for tenured positions should apply before January 18, 1988, while those applying at the Assistant Professor level have until February 29, 1988. For non-tenured appointments, if positions at this level remain unfilled, consideration may be given to applications received until May 1, 1988.

Computer and Information Sciences wishes to hire at the assistant professor level, with priority given to candidates with strengths in the areas of software engineering, programming languages and compiler construction (with emphasis on programming in parallel environments), and database languages (#77-867). A Ph.D. as above is required and applicants will be evaluated on their research record, teaching and professional activities. Apply before February 29, 1988. If position remains unfilled, consideration may be given to applications received until May 1, 1988.

Send curriculum vitae with cover letter, teaching evaluations, copies of any recent publications, and letters of recommendation evaluating your scholarly contributions, teaching, and other professional accomplishments to:

Chair, Computer Faculty Search Committee
Applied Sciences Building
University of California
Santa Cruz, California 95064

Please refer to a Provision # above when applying. All candidates should indicate citizenship and, in the case of non-US citizens, describe their visa status. The University of California is an EEO/AA/IRCA employer.

PRINCETON UNIVERSITY
Research Associate and Post-DOC

One or more research positions available immediately under several sponsored projects. The projects involve faculty, researchers and students, and cover the areas of databases, distributed systems, VLSI design, artificial intelligence, and computer architecture. Responsibilities include the design and implementation of software systems as well as their experimental evaluation. Ph.D with experience in at least one of the above areas is required. Salary open. Send resume to:

Hector Garcia-Molina
Department of Computer Science
Princeton University
Princeton, N.J. 08544

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ROSE-HULMAN INSTITUTE OF TECHNOLOGY
Faculty Position

Applications are invited for a tenure track position in the Department of Computer Science. Applicants should normally have a doctorate in Computer Science or a closely related discipline. Applicants should demonstrate both interest in and the potential for developing excellence in undergraduate teaching. Continued professional development and scholarly activity is also expected. Rank and salary will be commensurate with qualifications and experience.

Rose-Hulman Institute of Technology, located on a 300 acre campus near Terre Haute, Indiana, is a privately endowed school of engineering and science with 1300 carefully selected students. The Computer Science Department has five faculty members and offers a strong computer science program with considerable electrical engineering and mathematics content to approximately 100 Computer Science majors and some 25-30 EE/CS and MA/CS double majors. A graduate program at the masters level is planned for the near future. Computer facilities available to the department include a VAX 8530 with 40 terminals, two MicroVAX II's and numerous PCs. There are plans for a campus wide Ethernet as well as a local network of workstations in the Computer Science Department. About half of the student body own PCs.

Initial screening of candidates will begin February 1, 1988 and continue until the position is filled with appointment to be effective September 1, 1988. Send application and resume with three references to Prof. Frank H. Young, Rose-Hulman Institute of Technology, 5500 Wabash Avenue, Terre Haute, Indiana 47803. Rose-Hulman is an equal opportunity employer.

UNIVERSITY OF CALIFORNIA BERKELEY

THE UNIVERSITY OF CALIFORNIA AT BERKELEY invites applications for tenure-track positions in COMPUTER SCIENCE beginning in 1988-89. Applications for appointments at the ASSISTANT PROFESSOR level will be given highest preference, but other levels will be considered.

The Compuer Science Division of the Department of Electrical Engineering and Computer Sciences is strong and growing. We are interested in outstanding Computer Science candidates in all areas.

Research facilities include several mainframe computers (VAX 8600 and similar), numerous LISP machine (Symbolics, TI, Xerox) workstations, 80 general-purpose networked workstations (SUN and similar), and access to an on-site IBM 3090 and Cray-XMP. Instructional hardware includes numerous SUN workstations, VAX systems, Macintoshes, PC's and access to an IBM 3090.

A doctoral degree in Computer Science or a closely related field is required. Applicants should be able to teach core undergraduate courses and graduate courses. The successful candidate must have demonstrated outstanding research accomplishments. Send resume, a select subset on your best papers, and the names of three references by December 31, 1987, to the address below.

Professor Richard Fateman
Associate Chairman for Computer Science
Department of Electrical Engineering and Computer Sciences
University of California
Berkeley, CA 94720.

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UNIVERSITY OF CALIFORNIA, SANTA BARBARA

The University of California at Santa Barbara invites applications for at least four tenure track positions in the Department of Computer Science, effective 1988-89 academic year. These positions are available at all professorial levels, although the Department has a strong interest in appointments at senior levels. The Department of Computer Science is in a rapidly expanding College of Engineering, which has achieved great prominence in several areas of research. UCSB and the College of Engineering are highly committed to augmenting Computer Science in order to build a Department of great excellence and having national visibility. The Department is currently undergoing a major expansion, both in terms of faculty and facilities.

The positions currently available in Computer Science are in areas of research in which the Department intends to achieve its greatest strengths, namely Software Systems, Parallel and Distributed Computing, Machine Intelligence (particularly Computer Vision), and Scientific Computing. Senior appointments in these areas will provide opportunities for successful candidates to guide the growth and development of the Department. Resources will be available for state-of-the-art laboratories for research and instruction. Strong research support will be made available and tailored to the needs of successful applicants in these areas. Interactions with various research groups on campus, including the Center for Robotic Systems in Microelectronics, The Center for Computational Sciences and Engineering, The Institute for Theoretical Physics, and The Cognitive Science Program, will be strongly encouraged and supported. Applicants must possess a doctoral degree, and senior applicants must have an extremely strong record of research accomplishments. Teaching experience is desirable. Deadline for receipt of applications is *January 31, 1988.* Send resume and names of referees to:

Chairman, Planning and Recruitment Committee
Department of Computer Science
University of California
Santa Barbara, CA 93106

Proof of U.S. citizenship or eligibility for U.S. employment will be required prior to employment (Immigration Reform and Control Act of 1986). The University of California is an Equal Opportunity/Affirmative Action Employer.

UNIVERSITY OF WASHINGTON

The Department of Computer Science may have openings for tenure-track faculty appointments starting in the 1988-89 academic year. We are particularly interested in applicants with research strengths in artificial intelligence, databases, and programming languages and compilers. However, applications from outstanding individuals in other areas might also be considered. A moderate teaching load allows time for quality research and close involvement with students. We expect applicants to have a strong commitment to both research and teaching, and an outstanding record of research for their level. Any appointment should bring significant new research strength to the department.

The department may also have several visiting positions that would require both teaching and research. It may be possible to hold these for portions of the 1988-89 academic year.

Interested applicants should send a letter of application, a resume, and the names of four references to Paul Young, Chairman, Department of Computer Science FR-35, University of Washington, Seattle, Washington 98195.

The University of Washington is an Affirmative Action/Equal Opportunity Employer. The Ph.D. is required for these positions.

MEMPHIS STATE UNIVERSITY
Department of Mathematical Sciences

The Department of Mathematical Sciences invites applications for anticipated tenure track positions for 1988. The Department offers degrees at all levels including the Ph.D. and provides a very favorable research environment in terms of library and computing facilities (including a symbolic Intel Hypercube), teaching load, travel opportunities, etc. Preferred research areas in computer science include algorithms, parallel and distributive processing, artificial intelligence/cognitive science, software development, network design and analysis, and data communications. Preferred research areas in statistics include time series, biostatistics, engineering statistics, stochastic models, and applied statistics. Preferred research areas in mathematics include approximation theory, ergodic theory/dynamical systems, graph theory and combinatorics, ordinary and functional differential equations, linear and nonlinear functional analysis, and operator theory. Applicants must have a Ph.D. by September 1, 1988, and a strong potential for excellence in teaching and research.

Selection will begin on January 21, 1988. Applications will continue to be accepted until all positions are filled. Women and Minorities are strongly urged to apply. Successful candidates must meet Immigration Reform Act criteria. Applicants should submit a resume and direct three letters of reference to:

Ralph Faudree, Chairman
Department of Mathematical Sciences
Memphis State University
Memphis, TN 38152

An Equal Opportunity/Affirmative Action Employer.

THE AUSTRALIAN NATIONAL UNIVERSITY

Applications are invited for appointment to the position of POSTDOCTORAL FELLOW/RESEARCH FELLOW IN COMPUTER SCIENCES, DEPARTMENT OF ENGINEERING PHYSICS, RESEARCH SCHOOL OF PHYSICAL SCIENCES. Applications are sought for a full-time research position in the Computer Sciences Laboratory. The Computer Sciences Laboratory studies (1) parallel algorithms and architectures, including systolic arrays and transputer networks, (2) both fundamental and applied aspects of human-machine systems, including image analysis, speech recognition and speaker characterization. An interdisciplinary project involves information processing aspects of perception in biological systems. Applicants with a strong background in any related area of Computer Science are encouraged to apply. Further information may be obtained from Professor R P Brent. Closing date: 31 January 1988 Ref: PS.1.10.1 SALARY: Postdoctoral Fellow Grade 1 (fixed point); A $24,535-A $28,029 p.a.; Research Fellow; A $28,381- A $37,122 p.a.; APPOINTMENT: Research Fellow up to three years, possibility of extension to five years; Postdoctoral Fellow normally two years, possibility of extension to three years. APPLICATIONS should be submitted in duplicate to the Registrar, The Australian National University, GPO Box 4, Canberra ACT 2601, Australia, quoting reference number and including curriculum vitae, list of publications and names of at least three references. The University reserves the right not to make an appointment or to appoint by invitation at any time. Further information is available from the Registrar.

THE UNIVERSITY IS AN EQUAL OPPORTUNITY EMPLOYER.

THE UNIVERSITY OF TEXAS AT SAN ANTONIO
Director
Division of Mathematics, Computer Science and System Design

The College of Sciences and Engineering at the University of Texas at San Antonio is seeking a Director of the Division of Mathematics, Computer Science and Systems Design who will spearhead the continued development of excellence in the undergraduate and graduate programs. The division is the largest of four divisions within the college and is responsible for instructional programs, staffing, budget, planning supervision and curriculum.

Requirements: Candidates should have an earned doctorate in one of the disciplines encompassed in the division and should qualify for a senior level academic position. Successful teaching experience, demonstrated research record, and potential for administrative responsibility are requisites for the position.

To apply: Submit a letter of application and a vita with the names of at least three references to: Chairperson, Search Committee for Director, MCSSD, c/o Office of the Dean, College of Sciences and Engineering, the University of Texas at San Antonio, San Antonio, TX 78285. Nominations and/or applications will be accepted until January 15, 1988 or until the position has been filled.

The University of Texas at San Antonio is located among the hills and trees of the hill country in the northwest section of San Antonio. The first buildings on the 600-acre new university campus were opened for students in 1975 with an enrollment of nearly 5,000 students. Since then, the campus has grown and matured to a university of over 12,000 students in a wide variety of disciplines. The San Antonio region recognizes the importance of the University to its future growth and development.

The University of Texas at San Antonio is an equal opportunity/affirmative action employer.

UNIVERSITY OF MASSACHUSETTS AMHERST
Faculty and Research Scientist Positions

The Department of Computer and Information Science invites applications for tenure-track faculty positions and nontenure-track research scientist positions at all levels in all areas of computer science. Applicants should have a Ph.D. in computer science or related area and should show evidence of exceptional research promise. Senior level candidates should have a record of distinguished research. Salary is commensurate with education and experience. Our department has grown substantially over the past five years and currently has 28 full-time faculty, 18 research scientists, and 200 graduate students. Continued growth is expected over the next five years. We have ongoing research projects in robotics, vision, natural language processing, expert systems, distributed processing, database systems, information retrieval, software development, programming languages, computer networks, office automation, intelligent user interfaces parallel computation, and computer architecture. The department is the recipient of a CER award from NSF and URI award from ONR. To support our research, we have a 150-node network, including numerous large VAX and sequent systems, a variety of graphics devices, LISP Machines, and workstations. Send vita, along with the names of four references to: Professor Lori A. Clarke, COINS Department, Lederle Graduate Research Center, University of Massachusetts, Amherst, MA 01003, by April 1, 1988. An Affirmative Action/Equal Opportunity Employer.

UNIVERSITY OF SOUTHWESTERN LOUISIANA
The Center for Advanced Computer Studies
Research Faculty—Teaching Faculty
Graduate Fellowships/Assistantships in Computer Science/Engineering

The Center for Advanced Computer Studies is a research center with programs leading to MS/PhD degrees in Computer Science and Computer Engineering. External grants/contracts support research in a variety of areas. The Computing Research Laboratory includes a 40-node Sun-3 network, an Encore parallel processing system, 2 VAX 11/780s, logic development systems, laser printers, plotters, and other equipment. Instruction utilizes a 3-processor Pyramid 90X network running UNIX and an IBM 3090-200 with a vector processor. Another well-equipped facility supports research in CAD/CAM. About 300 students are enrolled in computing graduate programs, including 120 for the PhD. The undergraduate program in the Computer Science Department is accredited by CSAB and offers both scientific and commercial options, with a current enrollment of 610. The undergraduate program in the Electrical and Computer Engineering Department is accredited by ABET and offers an option in Computer Engineering, with a current enrollment of 250.

RESEARCH FACULTY: Applications are invited from persons holding PhD degrees with demonstrated research capabilities in Computer Science/Engineering. Persons appointed as Assistant Professors must hold PhDs in Computer Science/Engineering and have research potential. Associate Professors and Professors must hold PhDs and have an established research publication and grant record. The typical teaching load is 2 graduate-level courses per year and a continuing research seminar. Salaries range from $50,000 to over $100,000 per year. Excellent support for travel, equipment, research assistants, and professional activities is provided so you can achieve your professional goals. To apply, send a copy of your resume and the names and addresses of at least 3 professional references. Applications will be considered until all positions are filled.

TEACHING FACULTY: Tenure track positions are available for persons holding PhD degrees in Computer Science or Computer Engineering with a strong commitment to teaching undergraduates. Demonstrated interest and potential for performing limited independent research is desirable. Duties include teaching, advising, curriculum development, and program evaluation. Competitive salaries, support for travel, well equipped laboratories, and graduate assistant support provide an environment for quality instruction. To apply, send a copy of your resume and the names and addresses of at least 3 professional references. Applications will be considered until all positions are filled.

PhD FELLOWSHIPS: A number of PhD Fellowships valued at up to $18,000 per year are available. They provide support for up to 4 years of study towards the PhD in Computer Science or Computer Engineering. Recipients also receive preference for low-cost campus housing. Applications must be received by 15 February 1988.

MS/PhD ASSISTANTSHIPS: More than 100 teaching and research assistantships are available to support students pursuing an MS or PhD degree in Computer Science or Computer Engineering. Stipends are valued at up to $10,000 per academic year. Applications must be received by 1 March 1988.

APPLICATIONS: Dr. Terry M. Walker, Director, The Center for Advanced Computer Studies, Lafayette, LA 70504-4330. Phone: (318) 231-6284. *An Affirmative Action/Equal Opportunity Employer.*

UNIVERSITY OF MINNESOTA

Department of Electrical Engineering has several tenure track or tenured faculty positions in Electrical Engineering available at all levels. The duties will include research and teaching in one or more of the following areas: microelectronics, integrated circuit design, integrated optics, device physics, quantum electronics, research and applications of large scale computing, computer systems, control theory, digital signal processing and communications, computer-aided design and design automation, magnetics, electric energy systems and closely related specialties.

The Electrical Engineering Department has 45 faculty members providing undergraduate and graduate education and pursuing research in all areas of electrical engineering. The State-funded Microelectronics and Information Sciences Center and Supercomputer Institute at the University of Minnesota will provide opportunities for interdisciplinary research in cooperation with industry. The Department has a complete integrated circuit fabrication and design lab, access to Cray supercomputers, and other facilities.

A successful candidate is expected to establish a sponsored research program. The requirements include an earned Doctorate. Rank and salary will be commensurate with qualifications and experience. Temporary and visiting positions are also available. Send applications and resumes to:

Professor Michael Shur, Chairman of the Faculty Recruiting Committee
Department of Electrical Engineering, University of Minnesota
123 Church Street Southeast, Minneapolis, MN 55455

Last date for receiving applications: August 30, 1988, for positions available September 16, 1988. Review and interviews may begin as early as 11/15/87 and early decisions may be made on some positions.

The University of Minnesota is an equal opportunity educator and employer and specifically invites and encourages applications from women and minorities.

UNIVERSITY OF CALIFORNIA, SANTA BARBARA

University of California, Santa Barbara, Electrical and Computer Engineering. Applications are invited for tenure-track faculty positions, effective 7/1/88. Three positions are open for candidates experienced in millimeter-waves and microwaves; image processing; computer vision; or mutlivariable, robust, or fault-tolerant control system design. Two additional positions are anticipated for candidates with experience in computer engineering or optoelectronics. The positions start at the rank of Assistant Professor, although higher level appointments are possible for individuals with outstanding records. Normally, completion of a doctorate is required at the time of the appointment. Candidates should have an outstanding research potential or a distinguished research reputation, the ability to attract external research funding, and a strong commitment to teaching at the undergraduate and graduate levels. Applicants should send their resume and the names and addresses of at least four professional references, along with a brief statement of their research specialization to: Chairman, Faculty Search Committee, Department of Electrical and Computer Engineering, University of California, Santa Barbara, CA 93106, (805) 961-3821. Applications will be received until the positions are filled. Proof of U.S. citizenship or eligibility for U.S. employment will be required prior to employment (Immigration Reform and Control Act of 1986). An Equal Opportunity/Affirmative Action employer.

PURDUE UNIVERSITY
Computer Engineering Faculty Positions

The School of Electrical Engineering at Purdue University seeks outstanding candidates in all areas of Computer Engineering for research and teaching. Openings are for tenure-track faculty at all levels. Active research areas include artificial intelligence and expert systems; computer communication networks; computer vision; design automation tools; digital signal processor system design; distributed algorithms and databases; fault-tolerant and testable computing; microprocessor design; neural networks; parallel processing (architecture, algorithms, operating systems, compiling, languages, interconnection networks, and performance); robot vision, sensors and control; software engineering; speech processing; and VLSI architecture.

The School has over 70 full-time faculty (26 in Computer Engineering), and over $8M in funded research projects. In addition to the Ph.D., MSEE, and BSEE degrees, the School offers a BSCEE (Bachelor of Science in Computer and Electrical Engineering) which is accredited in both Computer Engineering and Electrical Engineering. Computing facilities available to the faculty include the Engineering Computer Network (including 17 VAX 11/780's running UNIX BSD 4.3, 4 Gould PN 9080's, a CCI PN 6/32, and 115 Sun workstations), the Computing Center's Cyber-205 supercomputer, a Symbolics LISP machine, extensive graphics facilities, and numerous PC's. Parallel computing facilities include a 128-node Ncube hypercube, a 48x48 processor NCR-GAPP processor array, a 10-processor Transputer array, the 30-processor PASM Parallel Processor prototype that was developed and built at Purdue, and the Computing Center's Sequent Balance 21000. Custom VLSI chip facilities include an IBM Master Image System. Equipment in the Robot Vision Lab and Computer Vision and Image Processing Lab includes a Puma 762 robot, a Cincinnati Milacron T3-726 robot, a K2A Cybermation mobile robot, and Gould/DeAnza, Comtal, Grinnell, and Imaging Technologies Image processing systems. Support facilities provided by the School include a technical typing pool and a graphics illustrator.

Applicants must possess a doctorate degree. Send a resume, including a statement of teaching and research interests and a list of at least three references to: Head, School of Electrical Engineering, Purdue University, West Lafayette, IN 47907. Purdue University is an Equal Opportunity/Affirmative Action employer.

HARVEY MUDD COLLEGE
Position Announcement In Computer Science

Applications are invited for a tenure track position In Computer Science at the Assistant Professor Level beginning July 1988. An applicant should have a Ph.D. in Computer Science and have a strong interest in both undergraduate teaching and research. Responsibilities include teaching, research, curriculum development, and the supervision of industrially-sponsored projects in computer science. The Computer Science Department's facilities include a network composed of a VAX 11/750 and a Sequent B21K. The Computer Science network is also interfaced with the college network of VMS machines: a Micro VAX 2, 4 VAX 11/750s and a VAX 8600.

Harvey Mudd College, one of the nation's most selective undergraduate colleges, is a member of the Claremont Colleges. The College is an equal opportunity/affirmative action employer. Please send resume and the names of four references to Professor Michael A. Erlinger, Chairman, Computer Science Search Committee, Harvey Mudd College, Claremont, CA 91711.

ARIZONA STATE UNIVERSITY
Computer Engineering
Computer Science

The Department of Computer Science in the College of Engineering at Arizona State University invites applications for tenure-track faculty positions at all levels. We presently have 29 faculty members, and we are seeking superior applicants in all areas of computer science and computer engineering. You must have or about to receive a Ph.D. in computer engineering or computer science or a related area, and you must show promise of excellence in teaching and research.

The state of Arizona, the university, and an impressive array of high-tech businesses in the Phoenix area are firmly committed to the continued development of outstanding programs in Computer Engineering and Computer Science at ASU. We have a new building with excellent office facilities, and another new building is being planned. ASU is in the Phoenix metropolitan area, which provides outstanding opportunities for joint work and professional development, and the nearby ASU research park provides additional opportunities.

Each faculty member has high-speed links to several networked computing facilities including 10 VAXes (750 through 8600, some with VMS and some with Unix), an NCUBE/7, a Harris HCX/7, 3 Harris 800s, an IBM 4381, an IBM 4341, and assorted other machines. An IBM 3081, over 100 Intel 310 stations running Xenix, and a large number of IBM PCs are also available.

Please send a resume and the names of three references by 31 January 1988 to Dr. David C. Pheanis, Search Committee, Department of Computer Science, Arizona State University, Tempe, Arizona 85287. AA/EOE.

INDIANA UNIVERSITY-PURDUE UNIVERSITY
At Indianapolis

The Department of Computer and Information Science invites applications for tenure track positions in all specialties. A Ph.D. in Computer Science or related field is required. Duties include research and six hours teaching. Rank and salary depend upon the candidate's qualifications. The positions are open until filled.

The Department is embarking on a significant expansion of its research efforts. Successful candidates will play a prominent role in this effort, as well as contribute to the growth of a major institution. The Department especially seeks individuals who will participate in its ongoing research in Applied Software and in Programming Languages.

The Purdue School of Science, in which the Department resides, is a major part of Indiana University-Purdue University at Indianapolis. IUPUI, a state university with an enrollment of over 23,000 students, has a mission to interact with the dynamic industrial community centered around Indianapolis. Its unique relationship with Purdue University at West Lafayette and Indiana University at Bloomington affords opportunities for joint research. The six-hospital Medical Center at IUPUI Is yet another source of cross-disciplinary research for the Department. Outstanding computing facilities Include a network of IBM, DEC, CDC and Prime machines.

Indianapolis itself has received national recognition as one of the best U.S. cities in which to live. Host of the 1987 Pan American Games, it enjoys numerous recreational and cultural activities, including a symphony, opera, and various theater groups. Its moderate cost of living and progressive civic leadership foster this rich environment.

Please send resumes and references to Dr. Andrew Olson, Chairman, Department of Computer & Information Science, Box 647, IUPUI, Indianapolis, IN 46223. IUPUI Is an Equal Opportunity/Affirmative Action Employer.

UNIVERSITY OF VICTORIA
Department of Computer Science

Applications are invited for tenure-track position as Assistant Professor to commence July 1, 1988. Applicants should have a Ph.D. In Computer Science or equivalent research achievement. The Department has sixteen full-time faculty, with several additional positions planned for the near future. It offers graduate and undergraduate degrees in Computer Science and maintains an active research program. The current research areas of interest are programming languages, compilers, software engineering, software development environments, distributed computing, combinatorial algorithms, theory of computation, logic programming, VLSI design and test, and numerical methods. The Department is an active participant in the Advanced Systems Institute of British Columbia.

The computing facilities available for instructional and research support currently include three SUN 3-280 systems, a VAX 11/780 and a Pyramid 90X, sixteen SUN workstations (four colour), microcomputer laboratories with a variety of small systems, as well as the University IBM 3083 system. A local area network provides convenient access to these facilities.

The city of Victoria, situated on the southern tip of Vancouver Island, has a population of over 200,000. It enjoys one of the most delightful environments in North America. The climate is temperate and all kinds of outdoor activities, from marine to mountain, are popular and can be pursued year round.

Applicants should send a curriculum vitae and the names of three referees to:

Dr. D.M. Miller, Chairman
Department of Computer Science
University of Victoria
P.O. Box 1700
Victoria, B.C., Canada
V8W 2Y2

Applications will be accepted until February 15, 1988. Further information is available through electronic mail (as indicated below) or from the Department, (604) 721-7220. Canadian immigration regulations now require the University to assess applications from Canadian citizens and permanent residents of Canada before those of others. The University of Victoria offers equal employment opportunities to qualified female and male applicants. Women are particularly encouraged to apply.

UUCP: {uw-beaver,ubc-vision}!uvicctr!dmill
BITNET: dmill@uvunix.bitnet
EAN: dmill@uvunix.uvic.cdn

OREGON STATE UNIVERSITY
Department of Computer Science

The Department of Computer Science invites qualified applicants for Assistant, Associate and Full Professors, tenure-track, nine-month to begin September 1988. Specialization in programming languages and systems, information-based systems, theoretical computer science, computer architecture, artificial intelligence or computer graphics is desirable. Applicants should have completed or expect to complete all requirements for a Ph.D. in computer science or a closely related field and should have demonstrated research and teaching potential. Candidates for senior positions should have an established research reputation. Review of applications will begin November 1, 1987, and will continue until the positions are filled. Please send resume, including the names of three references, to: Walter G. Rudd, Chairman, Department of Computer Science, Oregon State University, Corvallis, OR 97331.

Oregon State University is an equal opportunity affirmative action employer and complies with Section 504 of the Rehabilitation Act of 1973.

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Faculty Positions

The Department of Electricial Engineering and Computer Science seeks candidates for faculty positions starting in September 1988. We anticipate openings for several junior faculty appointments for individuals who are completing, or who have recently completed, a doctorate. Faculty duties include teaching at both the graduate and undergraduate levels, research, and supervision of theses.

We are interested in candidates in most areas of electrical engineering, but opportunities in bioelectrical engineering and microwaves are extremely limited at present. In computer science, we are interested in candidates in the following two areas: Computer Systems, Including operating systems, programming languages, computer architecture, databases, and graphics; and AI research in reasoning, including commonsense and qualitative physical reasoning, and reasoning using massively parallel machines.

All candidates should write to the address below, describing their professional interests and goals. Applications should include a curriculum vitae and the names and addresses of three or more references. Additional material describing the applicant's work, such as papers or technical reports, would also be helpful. All candidates should indicate citizenship and, in the case of non-US citizens, describe their visa status.

Send all applications to:

Prof. F. C. Hennie
Room 38-435
Massachusetts Institute of Technology
Cambridge, MA 02139

M.I.T. is an equal opportunity/affirmative action employer.

LOUISIANA STATE UNIVERSITY

Anticipated Faculty Position in Image Processing. The Department of Electrical and Computer Engineering and the Remote Sensing and Image Processing Laboratory at Louisiana State University invites applications for an anticipated faculty position. Ph.D. required in Electrical Engineering or Computer Engineering. The person would teach computer vision and computer engineering courses in the Department. Researh in computer vision would be conducted with the Remote Sensing and Image Processing Laboratory (RSIP). The position is attractive regarding a teaching load balanced to provide the ability to develop an academic program and provide time and resources for developing a high quality research program in computer vision. The RSIP Laboratory has well-qualified staff and modern computing and image processing equipment. A number of peripherals including Sun and International Imaging workstations are available. A comprehensive image processing system has been implemented in Berkeley Unix 4.3. The appointment will be made at a rank appropriate with the qualifications of the applicant. Verification of employment eligibility in compliance with the new Immigration Reform and Control Act is required. Interested applicants should apply by submitting a resume, statement of interests, and names and addresses of three professional references. Applications that apply by January 31, 1988 will be given preference. Apply to: Professor Charles A. Harlow, Director, RSIP Laboratory, 150 Electrical Engineering Building, Louisiana State University, Baton Rouge, Louisiana 70803-5901. LSU is an equal opportunity employer.

BILKENT UNIVERSITY

Faculty Positions

The Departments of Computer Engineering and Information Sciences, and Electrical and Electronics Engineering invite applications for several tenure track and visiting faculty positions at all levels in all areas. These Departments offer programs leading to B.S., M.S. and Ph.D. degrees. In addition to numerous micros, the departments have SUN workstations and a supermini computer. These departments are under constant expansion in terms of their sizes and facilities. Free furnished housing is provided on the campus. Applicants are expected to have a Ph.D. in related fields and a strong commitment to both research and teaching. The search remains open until positions are filled.

Please forward resume and 3 references to:

Dean
Faculty of Engineering and Science
P.O. Box 8
06572 Maltepe, Ankara
TURKEY
Telephone (90-4) 2664126 or 2664127

VANDERBILT UNIVERSITY

Electrical Engineering

Applications for faculty positions at all ranks in computer engineering are solicited from highly qualified individuals. Individuals will be selected primarily for their ability or potential to conduct research and to participate in a department committed to an expansion of its graduate, research and instructional programs. The School of Engineering is the oldest and largest private engineering school in the South. Vanderbilt is located in Nashville, TN, one of the South's most rapidly expanding metropolitan areas. Highly qualified applicants should send their resumes and the names of three references to: EE Search Committee, Electrical Engineering, Vanderbilt University, Box 1824, Station B, Nashville, TN 37235. Vanderbilt University is an Affirmative Action/Equal Opportunity Employer.

PROGRAMMERS-SCIENTIFIC

Tucson, Arizona

The National Optical Astronomy Observatories have a need at the National Solar Observatory for two Scientific Programmers to participate in the development of an image processing system for helioseismic data from the Global Oscillation Network Group project. Requirements for the Programmer I position include a M.S. in Computer Science or Astronomy; a minimum of three years of experience developing astronomy software; experience with solar image processing; one year of experience in IRAF task and application package development; and proficiency in FORTRAN, C, VAX VMS and SUN UNIX. Requirements for the Senior Programmer position include an M.S. in Computer Science, Mathematics, Engineering, or a Physical Science with a minimum of seven years professional programming experience designing, developing, and maintaining large software systems for image processing and for the management of large data volumes.

In an unclassified, sunbelt location, the NOAO offers an excellent compensation package including 24 days annual vacation and, after one year, a fully vested retirement plan. Please send your resume, in confidence, to: Judy Ruffino, Personnel Manager, National Optical Astronomy Observatories, P.O. Box 26732, Tucson, Arizona 85726.

An EE/AA Employer

CALIFORNIA STATE UNIVERSITY, HAYWARD

Department of Mathematics and Computer Science

The department is now seeking applicants for a tenure track Assistant Professor position in Computer Science beginning Fall, 1987.

Applicants should have the Ph.D. in Computer Science, or in a related field with computer science experience, and should have a commitment to excellence in teaching, willingness and ability to participate in curriculum development, and competence and potential for significant professional activities, including research and publication. All areas of specialization will be considered, but the areas of architecture, networks, software system design are particularly sought. The interests of the present faculty Include a wide range of theory, software design, and hardware design topics.

The Department of Mathematics and Computer Science enrolls nearly 1300 majors in its three degree programs; B.S. in Computer Science, B.S. in Mathematics, and M.S. in Mathematics. An M.S. in Computer Science is pending approval. The department has a Pyramid 90x minicomputer and four Sun3-160 color workstations connected on an Ethernet, a graphics lab, an Interactive classroom, a digital and a microprocessor lab, and numerous IBM PC's for faculty use. In addition, the campus has a Cyber 170, a FDP 11/44, a PRIME 9755, and several PC labs for student use.

Interested applicants should send a resume and the names of three references to:

Faculty Search Committee
Department of Mathematics and Computer
Science
California State University, Hayward
Hayward, CA 94542
e-mail: csuh!faculty-search@lll-crg.arpa

Applications received by January 20, 1988, will be assured full consideration. Applications will be accepted as long as the position remains available.

California State University, Hayward, is an Equal Opportunity/Affirmative Action employer and encourages applications from women and men of all ethnic backgrounds and physical abilities.

UNIVERSITY OF NEBRASKA-LINCOLN

Computer Science and Computer Engineering
Faculty Positions

Tenure-track positions in Computer Science and Computer Engineering are available with rank and salary open and preference given to Assistant Professors. Positions require a Doctorate in Computer Science, Computer Engineering or a related field and a strong commitment to research and teaching.

Expertise in any of the following areas are especially welcome: computer architecture, parallel processing, VLSI, operating systems, symbolic and algebraic computation, analysis of algorithms, artificial intelligence and programming languages.

The department has in place rigorous undergraduate and graduate programs through the Ph.D. in computer science and engineering research and education, and is expanding in the direction of computer engineering. The department offers degrees in two colleges, Arts and Sciences and Engineering and Technology. UNL provides a modern computing environment.

Applicants should submit vitae and names of three references by Janaury 4 to: Chairman, Search Committee, Department of Computer Science, 115 Ferguson Hall, University of Nebraska-Lincoln, Lincoln, Nebraska 68588-0115. Applications from women and minorities are especially encouraged.

Affirmative Action/Equal Opportunity Employer.

MORAVIAN COLLEGE
Computer Science Department

Qualified applicants in Computer Science and Information Systems are encouraged to apply for one and possibly two tenure track positions to begin September 5, 1988 at the assistant or associate professor level. An applicant is expected to be able to teach courses in an exciting, ACM-based, undergraduate program emphasizing software design and creative problem solving. Applicants in Computer Science should have special interests in analysis of algorithms, data structures, and theoretical foundations. An applicant in Information Systems is expected to possess a thorough background in software design techniques; to teach data base design, logical and physical system design; and to develop courses in expert systems. Computer Science students tend to be among the best at the school and number approximately 75.

A doctorate in computer science or equivalent discipline is preferred. Minimum requirement is a master's degree. In Information Systems, the doctorate is less necessary and background in software design together with otherwise strong credentials are suitable substitutes.

Moravian College is a selective, liberal arts and science college in the beautiful Lehigh Valley of Pennsylvania, 1 hour from Philadelphia and 1.5 hours from New York City. Based on a 4-1-4 calendar, the college is dedicated to excellence in teaching and supports a very high-quality CS program for its size of 1200 students. Founded in 1742, it is the sixth oldest college in the country. As a member of the Lehigh Valley Association of Independent Colleges, Moravian is engaged in a variety of cooperative programs with five other area institutions. The College's proximity to New York City, Princeton, and Philadelphia presents unusual opportunities for professional and cultural enrichment. Selection process begins February 15, 1988; applications will be accepted until the position is filled. A detailed resume should be sent to John P. Stoneback, Chair, Computer Science Department, Moravian College, Bethlehem, PA 18018. Moravian is an equal opportunity employer.

UNIVERSITY OF ALBERTA
DEPARTMENT OF COMPUTING SCIENCE

Applications are invited for two tenure-track positions at the Assistant/Associate Professor level. Responsibilities include research as well as teaching at the graduate and undergraduate levels. Strong candidates from all research areas will be considered, but areas of special interests include database systems, VLSI/computer architecture, operating systems, numerical analysis and computer graphics. Current hardware support includes an Amdahl 5870, a network of four VAX 11/780's and about thirty Sun Workstations, and well-equipped microcomputer and workstation laboratories for graphics, VLSI, and AI research. Access to a Cyber 205 is available. Salary is commensurate with qualifications and experience. Send curriculum vitae, names of three references, and up to three reprints or copies of important publications. New PhD's should also include a copy of their transcript. Apply to:

Dr. Lee J. White
Department of Computing Science
University of Alberta
Edmonton, Alberta
Canada
T6G 2H1

Applications will be accepted until January 31, 1988. The University of Alberta is committed to the principle of equity of employment, but in accordance with Canadian Immigration regulations, priority will be given to Canadian citizens and permanent residents.

NEW JERSEY INSTITUTE OF TECHNOLOGY
Computer and Information Science

Department seeks assistant, associate and full professors for spring/fall 1988. Ph.D. in computer science or closely related field required. Senior level applicants must have proven research and funding record. Positions available in, but not limited to: distributed computing including computer architecture, data communications networking, realtime computing and fault tolerance; software development including artificial intelligence, expert systems, computer graphics, office automation, data management systems, cognitive science, and computational linguistics.

Department offers B.S., B.A., M.S., and Ph.D., in computer science, and Ph.D. in management jointly with Rutgers-Newark. Computing facilities include VAX 8800, VAX 8530, IBM 4361, SUN workstations, Symbolics machines, TI Explorers and graphics systems.

NJIT is the comprehensive technological university of New Jersey with 7700 students enrolled in Newark College of Engineering, the School of Architecture, and College of Sciences and Liberal Arts.

Send resume and names of at least three references to:

Personnel Box CIS
New Jersey Institute of Technology
Newark, NJ 07102 EO/AA employer

NJIT does not discriminate on the basis of sex, race, color, handicap, national or ethnic origin, or age in employment.

WESTERN KENTUCKY UNIVERSITY
Head
Department of Computer Science

Applications are invited for the Computer Science Head position in the Ogden College of Science Technology and Health with an effective appointment date as early as June 1, 1988. The Department offers masters and baccalaureate programs in Computer Science with a current enrollment of approximately 300 majors. Applicants must hold a doctorate in Computer Science or a closely related discipline and have demonstrable administrative ability as well as experience in and a strong commitment to teaching; public service and scholarly activities. Review of completed applications will commence January 15, 1988. The position will remain open until filled. Submit a resume and the names of at least three references to: Office of Academic Affairs, Computer Science Head Search, Western Kentucky University, Bowling Green, KY 42101. An affirmative action, equal opportunity employer.

UNIVERSITY OF GENEVA (SWITZERLAND)
Faculty of Sciences
Department of Computer Science

Applications are invited for a tenure faculty position at the Full Professor level (or possibly Associate Professor level) starting October 1988.

Duties include research in computer science and applications, undergraduate and graduate teaching, thesis supervision and participation in administrative work.

A Ph.D. in computer science or a closely related discipline is required.

A good knowledge in French will be an asset.

Applications should be received by December 31st. 1987.

Please send resume, updated list of publications and the names of three or more references to

Doyen de la Faculté des Sciences
20 quai Ernest-Ansermet
1211 GENEVA 4 (Switzerland).

UNIVERSITY OF NORTH CAROLINA AT WILMINGTON

Applications are invited for a tenure-track position as Assistant/Associate Professor of Computer Science. Preferred specialties are: architecture and digital design, systems programming and operating systems, algorithms and complexity, graphics. Candidates should have a Ph.D. in Computer Science or Ph.D. in a related area with M.S. in Computer Science or equivalent experience. Duties include teaching, scholarship, and service. The Department has 30 faculty and offers B.S. in Computer Science and B.S., B.A. in Mathematics . VAX/VMS and UNIX are in use. For fullest consideration apply by February 1, 1988, to Douglas D. Smith, Chairman, Math. Sciences Department, University of North Carolina at Wilmington, Wilmington, NC 28403, (919) 395-3291. An EE/AA employer.

AUSTIN COLLEGE

Tenure-track position in computer science; salary and rank dependent on qualifications. Ph.D. in computer science or closely related field preferred; a master's degree or equivalent required. Applicants should have broad interests in various areas of computer science, and competencies in artificial intelligence and/or systems analysis are especially sought. In keeping with college's liberal arts philosophy, candidates should be willing to participate in college-wide interdisciplinary courses. Submit application by January 30, 1988 to: Dean David Jordan, Austin College, Sherman, Texas 75090. EOE.

STANFORD UNIVERSITY
Faculty Openings

The Departments of Electrical Engineering and Computer Science have a number of openings for regular and adjunct faculty and research positions. Applications are invited. Applicants should have a demonstrated research ability in one or more areas of computer hardware and software such as VLSI design, computer architecture, operating systems, or programming languages.

All applicants will be considered for positions beginning with the fall quarter 1987.

Stanford University is an affirmative action, Equal Opportunity Employer and welcomes applications from women and minority groups. Please submit, as soon as possible, a detailed resume, including references to Professor John Hennessy, Chairman, Search Committee, Computer Systems Laboratory, Department of Electrical Engineering, Stanford University, Stanford, California 94305.

ASTRONAUTICS TECHNOLOGY CENTER
Multiprocessor UNIX Development

Lead the development effort in multiprocessor operating system implementation for a supercomputer with unique architectural features. The individual we select will provide technical direction while working with an existing high-caliber design team to optimize architecture, compilers and the UNIX operating system in a multiprocessor environment.

The position requires in-depth knowledge of multi-user, multi-tasking and multiprocessor environments. UNIX expertise essential. The successful candidate must have the ability to perform and coordinate software development of advanced systems. PhD in Computer Science preferred. MSCS plus experience required. Send resume to:

ASTRONAUTICS TECHNOLOGY CENTER
5800 Cottage Grove Road
Madison, WI 53716
(608) 221-9001
Equal Opportunity Employer.

UNIVERSITY OF CONNECTICUT
Computer Science and Engineering

The Department of Computer Science and Engineering at the University of Connecticut is seeking a highly motivated and talented researcher and teacher to fill a tenure track faculty position at the Assistant, Associate or Professor level.

The Department offers B.S.E., M.S. and Ph.D. degrees in Computer Science within the School of Engineering. Women and minorities are actively encouraged to apply. Applicants must possess sufficient expertise in the computer architecture and digital systems areas to teach a hardware laboratory course. A demonstrated ability to perform leading edge research is also required, along with a mastery of the English language.

A full range of computing equipment including a CSNET link provides an environment conducive to research. The University is located in a rural area in northeast Connecticut within easy driving distance of several major metropolitan areas.

Applicants with Ph.D.'s in Computer Science, Computer Engineering or equivalent areas with an interest in joining an emerging department are invited to submit resumes and names of three references to: Lester Lipsky, Chair, Search Committee, Computer Science & Engineering Department, University of Connecticut, 260 Glenbrook Road, Box U-155, Storrs, CT 06268. We are an Affirmative Action/Equal Opportunity Employer, m/f. (Search #8A143).

UNIVERSITY OF CALIFORNIA, SAN DIEGO
Cognitive Science

The University of California, San Diego is considering the establishment of a Department of Cognitive Science and is seeking candidates for tenured or tenure-track positions at the Assistant Professor, Associate Professor, and Professor levels.

The Department will take a broadly-based approach to the study of cognition. It will be concerned with the neurological basis of cognition, individual cognition, cognition in social groups, and machine intelligence. It will incorporate methods and theories from a wide variety of disciplines including Anthropology, Computer Science, Linguistics, Neuroscience, Philosophy, Psychology, and Sociology.

We intend to develop a new curriculum for both undergraduate and graduate students and applicants should be interested in participating in the construction of new approaches to the study and teaching of cognition. We seek people whose interests cut across conventional disciplines. Interests in theory, computational modeling (especially PDP), application, and education are encouraged.

Candidates should send a vita, reprints, a short letter describing their background and interests, and names of at least three references to:

Search Committee
Cognitive Science, C-015-c
University of California, San Diego
La Jolla, CA 92093

Applications received prior to January 15 will be given the fullest consideration, however applications will be accepted until all positions are filled. Rank and salary will be commensurate with experience and qualifications, and will be based upon UC pay schedules.

Women and minorities are especially encouraged to apply. The University of California, San Diego is an Affirmative Action/Equal Opportunity Employer.

FAIRLEIGH DICKINSON UNIVERSITY
Assistant Professor of Computer Science

Fairleigh Dickinson University seeks an Assistant Professor of Computer Science for a full-time, tenure-track position on the Florham-Madison Campus beginning in September of 1988. The Florham-Madison Campus is located in the Northern New Jersey center of corporate research and development activity and is within 35 miles of New York City. Responsibilities include teaching of undergraduate and graduate computer science courses, student advising, scholarly research, and participation in the development of growing computer science programs.

Requirements: Ph.D. in computer science, or within one year of completion of such a degree. Teaching experience is preferred.

Salary: Competitive and commensurate with qualifications and experience. Submit resume and letter of application to: FAIRLEIGH DICKINSON UNIVERSITY, University Employment Office, 285 Madison Avenue, Madison, New Jersey, 07940. Attention: Professor Peter Falley, Chair, Department of Math/CS/Physics. Letters of applications and resumes will be accepted through March 31, 1988 or until the position is filled.

FDU, serving approximately 14,000 students on three main campuses, is the largest private university in New Jersey.

Equal opportunity/affirmative action employer.

CLEVELAND STATE UNIVERSITY

TENURE-TRACK FACULTY: The Department of Computer and Information Science at Cleveland State University has a tenure-track position at any level to begin Fall, 1988. Responsibilities include teaching (two courses/quarter) & research participation. Salary is very competitive. Qualifications: Ph.D. in Computer Science, MIS, Computer Engineering, or a closely related field. For instructor positions, Ph.D. candidates with some or substantial progress on a dissertation will be considered. Close relationships to business, engineering, science, and other departments provide an environment conducive to research and consulting. In addition to university computing facilities, the department provides its own laboratories using VAX and other computers running UNIX and VMS and state-of-the-art software for faculty and students. Faculty offices are equipped with personal computers. Inquiries and vita should be sent to: Dr. Thomas S. Heines, Chairperson, Computer & Information Science Dept., Cleveland State University, E. 24th & Euclid Ave., Cleveland, OH 44115. EOE, m/f/h.

LOUISIANA STATE UNIVERSITY
Computer Faculty Positions

The Department of Electrical and Computer Engineering at LSU invites applications for anticipated tenure-track and visiting faculty positions available August 1988 in all areas of computer engineering, including microprocessors, distributed processing systems and special purpose architectures. A Ph.D. or equivalent and potential for excellence in teaching and research are necessary. Rank is open. Salary is competitive and commensurate with qualifications and experience. Release time and resources are provided in order to enhance the development of a quality research program. Opportunities for summer support are available. Send resume, names of three references, verification of employment eligibility in compliance with the new Immigration Reform and Control Act, and a statement of teaching and research interests to: Alan H. Marshak, Chairman, Electrical and Computer Engineering, Louisiana State University, Baton Rouge, LA 70803-5901. LSU is an Equal Opportunity Employer.

UNIVERSITY OF NORTH CAROLINA AT CHARLOTTE
Department of Computer Science

Several tenure-track positions in all areas at Assistant, Associate, or Full Professor level in Computer Science/Computer Engineering. Salary and rank dependent on qualifications and experience. Salary is competitive. Ph.D. in CS/CE preferred. Ph.D. in a related area to CS/CE considered. Applications accepted until the positions are filled. The Department of Computer Science is housed in the College of Engineering and offers both undergraduate and graduate degrees in computer science. Active research areas in the department include artificial intelligence, computer architecture, computer vision/robotics, database systems, data communication, theoretical CS, VLSI design. On-campus Ph.D. level research and study are available through cooperation with other participating institutions of the Microelectronics Center of N.C. (MCNC). A wide variety of excellent computing facilities including IBM, VAX, Burroughs, Harris, Xerox, Sun, and others are available to support educational and research activities. Also, as a participant in MCNC, UNCC has access to state-of-the-art computing, VLSI design, and fabrication facilities. Charlotte is the largest city in the Carolinas with excellent housing, good schools and mild climate.

Vita, transcript and four letters of reference should be sent to Chairperson, Faculty Search Committee, Department of Computer Science, The University of North Carolina at Charlotte, Charlotte, NC 28223.

UNCC IS AN EOE/AA EMPLOYER

PORTLAND STATE UNIVERSITY
Computer Science Department

The Department of Computer Science has tenure-track faculty positions at the Assistant, Associate or Full Professor level available immediately. Thanks to support provided by local high-tech industries, we are able to offer competitive salaries and working conditions.

Applicants must have an earned doctorate. Responsibilities include undergraduate and graduate teaching, development of sponsored research and interaction with local industry.

PSU's Computer Science Department is located in the Portland Center for Advanced Technology, which houses both the Electrical Engineering and Computer Science departments, plus CAD/CAM, VLSI design, computer vision and optical communications laboratories. The CS department has SUNs and several other UNIX and AI machines including extensive equipment gifts from local companies.

Portland has a rapidly growing computer and electronics industry including a branch of Intel and the world headquarters of Tektronix, Floating Point Systems, Servio Logic, Sequent Computer Systems, Metheus, Mentor Graphics and Oregon Software, permitting close industry-university interaction.

Send applications, including a resume and the addresses of three references, to:

Dr. Leonard Shapiro
Department of Computer Science
Portland State University
P.O. Box 751
Portland, OR 97207
Telephone: (503) 464-4036

Deadline for applications is February 1, 1988 or thereafter until the position is filled. Non-U.S. Residents must state their visa status. Portland State University is an equal opportunity/affirmative action employer. Qualified minorities, women, and members of other protected groups are encouraged to apply.

THE UNIVERSITY OF MICHIGAN
Division of Computer Science and Engineering

The Department of Electrical Engineering and Computer Science at The University of Michigan invites applications for tenure-track positions in its Division of Computer Science and Engineering. As the consequence of a recent merger of computer faculty from two departments, research and teaching in computer science/engineering is now concentrated in a single division which currently has 33 faculty members. Located in a new building on the North Campus and with a strong commitment from the University, the Division is entering an exciting period of further expansion, particularly in the areas of software systems, hardware and architecture, artificial intelligence and robotics.

Openings in the software area are at all levels and cover a broad range of specializations including software engineering, operating systems, languages, performance evaluation, distributed systems, computer networks, alternate programming paradigms, and computer graphics. Strong programs are already in place in hardware, architecture, and fault-tolerant computing, and we seek further expansion with junior level positions in areas of parallel processing, multiprocessing, real-time systems, computer-aided design, performance-reliability evaluation, and VLSI systems design. Currently active programs in artificial intelligence include machine learning, natural language understanding, and machine vision. In AI, we seek at least one senior faculty member with fundamental interests that underlie these ongoing programs. The robotics program, which has grown considerably in recent years, is likewise seeking additional faculty, particularly in areas of task planning, mobile robots, and sensing. All candidates who apply should have an interest in teaching and a strong research orientation.

Send your resume and the names of at least three references to Professor Keki B. Irani, Associate Chairman, Division of Computer Science and Engineering, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, Michigan 48109-2122. The University of Michigan is an Equal Opportunity/Affirmative Action Employer.

TEXAS A&M UNIVERSITY
Department Head, Computer Science

Texas A&M University invites applications and nominations for the position of Head of the Department of Computer Science in the College of Engineering. The Department of Computer Science conducts an educational and research program embracing major technical specializations of the profession. The Department offers degrees at bachelors, masters, and doctoral levels and currently has approximately 1,100 students of which 150 are graduate students.

The candidate should hold a Ph.D. degree or equivalent in computer science, computer engineering, electrical engineering, or a related field and be nationally recognized in his or her field. The Head also holds the rank of Professor of Computer Science with tenure. Salary is negotiable. Applicants should send a vita and the names, addresses, and phone numbers of three references to Professor Kemble Bennett, Chairman, Computer Science Department Head Search Committee, Department of Industrial Engineering, Texas A&M University, College Station, TX 77843. Phone (409) 845-5502.

Applications will be accepted until the position is filled. Screening will begin on January 4, 1988. Texas A&M University is an Equal Opportunity/Affirmative Action Employer. Women and minorities are encouraged to apply.

UNIVERSITY OF CALIFORNIA
SAN DIEGO

The Department of Computer Science and Engineering invites applications for computer science and computer engineering faculty positions (tenure track) involving research and teaching at both graduate and undergraduate levels. The department and the university offer an outstanding environment for academic computer science. We are interested in strong candidates from all major areas of computer science (except numerical analysis). For appointment at the assistant professor level, evidence of excellent potential for conducting research in computer science is necessary. For senior level appointments, exceptional research accomplishment in computer science is required. Salary and rank will be commensurate with qualifications in conformance with University of California policies; a Ph.D. in computer science is required. Applications received by January 31, 1988 will be considered for all positions, but later applications will also be considered if unfilled positions remain. Please send a curriculum vitae and the names of four references to: Dr. Walter A. Burkhard, Dept. of Computer Science and Engineering, Mail Code C-014, University of California, San Diego, La Jolla, California, 92093. UCSD is an Equal Opportunity/Affirmative Action employer.

WASHINGTON UNIVERSITY
St. Louis
Regular Faculty Positions in Computer Science

The Department of Computer Science at Washington University in St. Louis is expanding its research program and invites applications for regular (tenure-track) faculty positions at the Assistant, Associate and Full Professor levels. Applicants should hold the Ph.D. or D.Sc. degree in Computer Science and have a strong commitment to and record of accomplishment in research.

The Department of Computer Science has a well-respected undergraduate program and a growing graduate program. Research activities have flourished in recent years and have three foci: concurrent systems, communications systems, and intelligent computer systems, with an emphasis on the use of visualization as a tool in each case. Support for these research programs is from NSF, NIH, ONR, DMA and a large number of industrial sponsors.

Current departmental research in concurrent systems includes the formal foundations of concurrent computation, programming languages and methodologies for the design of concurrent systems, system interconnection networks and parallel architectures and algorithms. The department is also engaged in research on the design of fast packet-switching systems capable of a variety of applications (including voice, data and video). Of particular interest are candidates with backgrounds in communications systems architecture, communications software, or performance analysis. In the area of intelligent computer systems, present research projects include computer vision, image processing, visual programming, speech recognition, expert systems and deductive databases. Individuals with backgrounds in any of these areas are encouraged to apply.

Qualified applicants may send a vita and names and addresses of at least three references to Dr. Jerome R. Cox, Jr., Chairman, Department of Computer Science, Washington University, Campus Box 1045, St. Louis, Missouri 63130. Applications are requested by February 1, 1988. Washington University is an equal opportunity/affirmative action employer.

PORTLAND STATE UNIVERSITY

The Department of Electrical Engineering has tenure-track faculty positions at the Assistant, Associate, or Full Professor level. Applicants must have an earned doctorate and demonstrated research expertise in an electrical engineering field. Areas of particular interest are Computer Engineering, Computer Graphics and Architecture, Integrated Circuit Design and Device Modeling, Communications, Systems and Controls, Power Electronics, Computer Vision and Electromagnetics. A VLSI design center, computer vision and graphics laboratories, and a laser laboratory have recently been established in the Portland Center for Advanced Technology. Faculty members have access to a departmental network of VAXes and Sun workstations as well as university IBM and Gould computers. Responsibilities include undergraduate and graduate teaching, development of sponsored research, and interaction with local industry.

Portland State University is one of the three major universities in the Oregon State System of Higher Education. It is located in Portland, Oregon with easy access to the well known recreational opportunities of Oregon's mountains, rivers, and coast. The Department of Electrical Engineering offers B.S., M.S., and Ph.D. degrees in electrical and computer engineering. The Department has 12 full-time faculty and over 200 students admitted to its upper division and graduate programs.

Portland has a rapidly-growing computer and electronics industry including Tektronix, Intel, Hewlett-Packard, Floating Point Systems, Electro-Scientific Industries, Northwest Instruments, Sequent Computer Systems, Metheus, Mentor Graphics, Oregon Software, Lattice, and others, which permits close industry-university interaction.

Rank and salary are commensurate with qualifications and experience. Send an application, including a resume listing the names of three references to: Dr. Lee W. Casperson, Head, Department of Electrical Engineering, Portland State University, Portland, Oregon 97207-0751. Phone: (503) 464-3806. Applications will be accepted until February 1, 1988, or until suitable candidates are identified.

Non-U.S. residents must state their visa status. Portland State University is an equal opportunity/affirmative action employer.

THE UNIVERSITY OF MICHIGAN
ANN ARBOR, MICHIGAN
Faculty Positions Available in Electrical Engineering and Computer Science

Applications are solicited for faculty and research scientist positions at all ranks in various areas of electrical engineering and computer science and engineering. Qualifications include an outstanding academic record, significant involvement in research, a doctorate in electrical or computer engineering or computer science, and a strong commitment to teaching and research. Areas of specialization being considered are artificial intelligence, circuits and microelectronics, communication networks, computer architecture, image processing, languages and compilers, millimeter-wave antennas and remote sensing, operating systems, optics, robotics and integrated manufacturing software engineering, solid-state devices, VLSI.

Please send resumes to:

Chairman
Department of Electrical Engineering and
Computer Science
The University of Michigan
Ann Arbor, MI 48109-2122

An Equal Opportunity/Affirmative Action Employer.

CENTRAL MICHIGAN UNIVERSITY
Department of Computer Science

Applications are invited for tenure-track faculty positions beginning Fall 1988. These positions are targeted at the assistant professor level, though all ranks will be considered. Applicants should have a Ph.D. in Computer Science or a related area and a commitment to excellence in teaching and research. All fields of Computer Science will be considered, but preference will be given to individuals with interests in Operating Systems, Database Management, Programming Languages, Artificial Intelligence, and Computer Architecture. Benefits are excellent and salary is competitive and commensurate with experience. Duties include teaching 6-9 hours per semester.

The Department offers B.S. and M.S. degrees in Computer Science. The departmental computational facilities include a VAX 8530, Burroughs XE-550 and several microcomputers. In addition, access to an IBM 3090/150E (a university facility) is also available. A graphics and image processing laboratory is currently being upgraded.

Central Michigan University is a state-supported institution with an enrollment in excess of 16,000 students. The City of Mt. Pleasant has a population of 24,000 and has many of the advantages of a big city without the congestion, being sixty miles north of the state capital of Lansing.

Please send a detailed resume and three letters of references to:

Prof. S. N. J. Murthy, Chair
Department of Computer Science
Central Michigan University
Mt. Pleasant, MI 48859
(Tel: 517-774-3774).

Central Michigan University is an Equal Opportunity/Affirmative Action employer.

YALE UNIVERSITY
Electrical Engineering

The Department of Electrical Engineering invites applications for a junior faculty appointment in VLSI system design, computer architecture, parallel processing and other areas of computer engineering. Applicants should have a Ph.D. in Electrical Engineering, Computer Science, or closely related field, and should exhibit outstanding research accomplishments or potential. Send resume, including names and addresses of at least three references, to Professor Peter M. Schultheiss, Chairman, Department of Electrical Engineering, Yale University, P.O. Box 2157 Yale Station, New Haven, CT 06520. Yale University is an affirmative action, equal opportunity employer.

UNIVERSITY OF MINNESOTA, DULUTH

The College of Science and Engineering is seeking candidates for an endowed professorship in engineering. The appointee will have responsibilities for teaching, research and development. Minimum qualifications are a baccalaureate in appropriate science or engineering field with 10 years experience. A Ph.D. appropriate to the science or engineering field with 20 years industrial and academic experience is preferred. Salary is negotiable and competitive. Completed applications must be received no later than 1 February 1988. For additional information contact: Jack Rowe Professorship, Search Committee, Attn: James Johnson, Chair, College of Science and Engineering, 140 Engineering Bldg., 10 University Dr., Duluth, MN 55812 USA. The University of Minnesota is an equal opportunity educator and employer and specifically invites and encourages applications from women and minorities.

UNIVERSITY OF CALIFORNIA, IRVINE
Computer Engineering Area

The Department of Electrical Engineering at the University of California, Irvine, invites outstanding individuals to apply for tenure track positions at all levels in the area of computer engineering. The positions will be filled by June 30, 1988. The levels of these appointments may be at Assistant Professor, Associate Professor, or Professor depending on accomplishments and stature in the field. Subareas of special interest include. but are not limited to:

1. Advanced computer architecture e.g., distributed architectures, highly parallel architectures, ultra-reliable architectures, inference machine architectures, and applications-oriented architectures.
2. System software including operating systems.
3. Advanced applications of computer engineering including computer communications, artificial intelligence, etc.

Responsibilities include research and teaching at the graduate and undergraduate levels.

The Department has research activities in design automation, VLSI design, distributed computing, fault-tolerant computing, and real-time computing, and in closely related areas including digital signal processing, image understanding, robotics, digital communication, and communication networks. The Department currently has nineteen faculty members, two of whom are members of the National Academy of Engineering and seven are Fellows of the IEEE. Send your complete resume with a list of at least three references to Kane Kim, Chairman of the Computer Engineering Faculty Search Committee, Department of Electrical Engineering, University of California, Irvine, California 92717. The University of California is an affirmative action/equal opportunity employer. Although applications will be accepted until the positions are filled, apply before February 15, 1988 to ensure being considered. Early applications are encouraged.

THE STATE UNIVERSITY OF NEW YORK AT BUFFALO
Director of Academic Computing

The State University of New York at Buffalo (SUNY-Buffalo) is seeking applications for the position of Director of Academic Computing. The person is responsible for developing and coordinating computer services in support of instruction and research, and for providing leadership and direction for SUNY-Buffalo's growing academic computing activities. The Director of Academic Computing reports to the Associate Vice President for Computing and Information Technology.

Qualifications: The position requires a master's degree in a science related field, although a Ph.D. degree is highly desirable. The successful candidate will have demonstrated experience in an administrative and management profession with an excellent grounding in current trends in Academic Computing, and an enthusiasm for developing new and innovative approaches to delivering computing services.

Applications from members of minority groups and women are encouraged. Applications, curriculum vitae and names of three references should be submitted to:

Chairperson, Academic Computing Search Committee
305 Computing Center, Box 7
State University of New York at Buffalo,
Buffalo, New York 14260
Screening begins November 15, 1987.
SUNY/Buffalo is an Affirmative Action Equal Opportunity Employer

THE UNIVERSITY OF RHODE ISLAND
Assistant Professor, Computer Engineering

Tenure track position requiring a Ph.D. in Electrical or Computer Engineering or Computer Science with one or more areas of specialization such as LSI/VLSI design, computer architecture, artificial intelligence, computational complexity, real-time computing, fault-tolerant computing, parallel processing or computer networks. Computing is supported in the department by a DG MV10000, VAX 11/780, Eclipse S250, LSI-11 and a microcomputer laboratory and on campus by an IBM 4381 mainframe and two PRIME 9955 minis. Submit letter of application and resume by December 31, 1987 (applications will be accepted until the position is filled) to: Assistant Professor Computer Engineering Position, THE UNIVERSITY OF RHODE ISLAND, P.O. Box G, Kingston, RI 02881. An Affirmative Action/Equal Opportunity Employer.

THE UNIVERSITY OF TENNESSEE
Department of Computer Science
Knoxville, Tennessee 37996-1301

The Department of Computer Science invites applications for tenure-track and visiting positions at all ranks beginning Winter of 1988. A doctoral degree in computer science or a related area, and a strong interest in research in the areas of computer networks, computer graphics, and operating systems are required. Those with experience directing doctoral students are especially encouraged to apply.

The department operates a research laboratory which contains two DEC VAX-8200's (one VMS, one UNIX) and a variety of microcomputers. Each faculty member has a personal workstation. Specialized laboratories support research in areas of special emphasis. The University of Tennessee Computing Center operates an IBM 3081, an IBM 4381, and a cluster of VAX 8600's. Faculty members collaborate with scientists at the Oak Ridge National Laboratory and frequently have access to their facilities, including a Cray X-MP and hypercube computers, under the terms of the collaboration. Faculty workstations are networked with the departmental laboratories, the University Computing Center, and facilities at the Oak Ridge National Laboratory.

You can respond on CSNET with csnet:straight @utenn and on BITNET with bitnet:straight@ utkcs1. The mailing address is Computer Science Department, 107 Ayres Hall, The University of Tennessee, Knoxville TN 37996-1301.

The University of Tennessee is an EEO/TITLE IX/SECTION 504 employer.

UNIVERSITY OF CENTRAL FLORIDA
Research Associates

The Institute for Simulation and Training located at the University of Central Florida is seeking qualified applicants to fill the positions of Research Associate—Computer Science, and Program Director—Computer Science/Artificial Intelligence. Openings starting in February 1988. Doctorate in Computer Science, Engineering or discipline related to simulation and training. Experience in integrating systems and systems architecture required. Experience in mathematical modeling and/or significant experience with artificial intelligence including knowledge presentation and natural language presentation. Salary $45,000 to negotiable. Send resume to A.L. Medin, Director, Institute for Simulation and Training, University of Central Florida, Orlando, Florida 32816. Equal Opportunity Employer. As an agency of the State of Florida, UCF makes all search records open to the public.

GEORGIA INSTITUTE OF TECHNOLOGY
School of Information and Computer Science

The School of Information and Computer Science invites applications for faculty positions at all levels. Applicants should have a commitment to teaching and a record of outstanding research accomplishments. Applicants who expect to receive a Ph.D. degree by Fall 1988 and who show high potential for research as well as a commitment to teaching are also invited.

The School seeks applicants to strengthen its capabilities in all areas of current research activity, especially artificial intelligence, software engineering, distributed computer systems, and also in computer graphics, programming languages, theoretical computer science, human factors, VLSI systems, data communications and computer networks, database systems, and computer architecture. Very competitive salaries are offered.

The School has 27 faculty members and anticipates further faculty growth. Its educational activities include an undergraduate program accredited by the Computing Sciences Accreditation Board, Inc., a Masters program with 150 students and a Ph.D. program with over 70 students. Well equipped laboratories support research and education. For instance, a recently established programming laboratory features a network of twenty-four Unix-based workstations. High-speed local area networks interconnect all major campus laboratories and provide access to national newtworks.

The School has been named a 1987 recipient of a five year Coordinated Experimental Research grant from the National Science Foundation. This grant will fund acquisition of hardware and development of software to support experimental work in parallel and distributed computing.

Georgia Tech is located in Atlanta, which experiences a mild sunbelt climate. It is the center of commerce in the Southeast, offering a diverse economy and good employment opportunities in all professional areas. Atlanta offers good cultural and recreational opportunities, extremely attractive residential neighborhoods, and affordable housing.

Candidates should send complete resumes and names of at least three references to: Professor Richard J. LeBlanc; Chairman, Faculty Search Committee; School of Information and Computer Science; Georgia Institute of Technology; Atlanta, Georgia 30332.

Georgia Tech is an equal opportunity employer.

UNIVERSITY OF HOUSTON

Applications are invited for tenure track faculty positions in the Department of Computer Science starting September 1988. Areas of special interest include but not limited to artificial intelligence, computer architecture, operating systems, programming languages and software engineering. Rank and salary are open and competitive. The Department is interested in expanding its research program and particularly welcome applicants for senior positions. Applicants should have a Ph.D. in Computer Science or a closely related area, and a strong commitment to research and teaching. Candidates for senior positions should also have a distinguished research record. The Department offers Ph.D., M.S., and B.S. in Computer Science. Departmental research facilities include a network of SUN Workstations, VAX 11/780 and VAX 11/730's, a network of AT + T 3B20 and 3B2's and access to other computing facilities in the University Computer Center as well as supercomputers via remote access terminals. Send resume and names of professional references to Dr. Willis King, Chairman, Department of Computer Science, University of Houston, Houston, Texas 77004. An Equal Opportunity/Affirmative Action Employer.

NATIONAL SCIENCE FOUNDATION (NSF)

NSF's Division of Information, Robotics, and Intelligent Systems (IRIS) is seeking qualified applicants for the position of Program Director, Robotics and Machine Intelligence Program. The individual selected for this position will administer a grant program in support of research in Robotics and Machine Intelligence. The position will be filled on a one- or two-year rotational or temporary basis and is excepted from the competitive civil service.

Alternatively, the assignment will be made under the provisions of the Intergovernmental Personnel Act (IPA). Salary ranges from $45,763 to $72,500* (*current statutory limit). The rotator candidate receives a leave of absence from his/her employer and salary is set in accordance with NSF's, Rotator Program.

Applicants must have a Ph.D. or equivalent professional experience and training in information or computer science/engineering or a related field. In addition, 5 or more years of substantial scientific research experience beyond the Ph.D. is required. A broad general knowledge of information and computer research and some administrative experience is also required.

Applicants should send resume or SF-171, Application for Federal Employment, to: National Science Foundation, 1800 G St., NW., Room 208, Washington, DC 20550. Attn: Catherine Handle (202) 357-7840. Hearing impaired individuals should call (202) 357-7492.

For technical information about the position, contact Dr. Y.T. Chien, (202) 357-9572 or by net mail to YTCHIEN@NOTE.NSF.GOV). NSF is an Equal Opportunity Employer.

UNIVERSITY OF MINNESOTA
Computer Science Department

The Computer Science Department at the University of Minnesota invites applications for regular, visiting, temporary and adjunct faculty positions at all ranks and in all areas of computer science. The department also has distinguished professorships available. All regular faculty positions require an earned doctorate, and involve teaching, research and service. Assistant Professors must have demonstrated research and teaching ability. For tenured Associate and Full Professorship positions, candidates must have demonstrated effectiveness in teaching and attained a reputation in scholarly research. For Associate Professorships, a minimum of three years teaching and research is required; for full professorship a minimum of six years teaching and research is required or an appropriate combination of these. An adjunct appointment at any rank requires professional accomplishments equivalent to those required for an appointment as a regular faculty member at the same rank.

Non-regular positions as teaching specialists, lecturers, and postdoctoral fellowships are also available. Candidates for lecturer must have an earned doctorate, and candidates for teaching specialist must have a Master's degree in computer science or related fields.

While applicants from all areas of computer science are sought, we are especially interested in applicants with strong research interests in the following areas: artificial intelligence, robotics, computer architecture, computer graphics, operating systems, software engineering, software systems, large scale scientific computing, and supercomputing.

Minnesota is a major center of the computer industry. The Computer Science Department currently has 26 full-time faculty and numerous adjunct faculty. The activities of the department are augmented by the activities of the Minnesota Supercomputing Institute, the Microelectronics and Information Sciences Center, the Institute for Mathematics and its Applications, and the Charles Babbage Institute for the History of Information Processing. University-wide computing facilities include a CRAY-2, a CYBER 205, an ENCORE Multimax, and several other CYBERs and VAXs. The department of Computer Science operates a VAX-11/780, Data General MV-10000, clusters of SUN and HP workstations, a network of Apollo workstations, and a 64 node NCUBE hypercube computer. The department is on CSNET, ARPANET, and UUCP networks.

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Applicants should send their resume and the names of at least four references to:

Professor David Fox, Chair, Faculty Search Committee, Computer Science Department, 136 Lind Hall, University of Minnesota, 207 Church Street SE, Minneapolis, MN 55455.

The University of Minnesota is an equal opportunity educator and employer and specifically invites and encourages applications from women and minorities.

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The Computer Science Department invites applications for a tenure-track position starting September, 1988. Ph.D. in Computer Science or in a closely related field is required. There is need to staff the mainline undergraduate courses and to strengthen the masters' program. For more information, please contact James Johnson, Chair; Computer Science Dept.; Western Washington University; Bellingham, Washington 98225. CSNET address: johnson@wwu.edu. Applications will be taken until March 20, or until the position is filled. WWU is an EO/AA employer.

BOOK REVIEWS

Editor: Wiley McKinzie, School of Computer Science and Technology, Rochester Institute of Technology, Rochester, NY 14623; Compmail, w.mckinzie; CSnet, wrm@rit

Data Communications and Teleprocessing Systems, Second Edition

Trevor Housley (Prentice-Hall, Inc., Englewood Cliffs, N.J., 1987, 474 pp., $33.50)

There is an ever-increasing demand for communication between terminals and computers located at different sites, as well as between computers themselves. However, lack of standardization has produced a wealth of strange and conflicting terminology. Mr. Housley's book makes this complex world easier for beginners.

The first six chapters of the book introduce the reader to the world and concepts of data communication. These chapters define data communications processes such as half- and full-duplex transmission, and explain the function and operation of devices such as multiplexers, terminals, front-end processors, controllers, and modems. The author uses effective, everyday examples. To show how half-duplex transmission works, for instance, he compares it with a one-way street that may carry traffic in one direction at certain times and in the opposite direction at others. He compares full-duplex transmission with a two-way street. He provides pictures to assist the explanation of the different kinds of terminal operation.

Subsequent chapters are more useful for engineers who have to deal with the management of computational resources. These chapters provide valuable information on how to tackle problems of data communications via modem with multiplexers, controllers, front-end processors, and all varieties of terminals. The interested reader will also find some information on network analyzers, the information that these devices can provide, and how to use them for good network management.

Personally, I think Mr. Housley's book is best when dealing with data communication problems via modem. It provides several examples of how to connect terminals to controllers and front-end processors. These examples can be applied to the solution of actual design problems.

The book also provides less extensive, complementary discussions of telephone networks, facsimile, integrated services digital networks, and local area networks.

One minor shortcoming is the lack of any explicit reference material on the subjects covered in the book. A more serious shortcoming is the way two very interesting examples, namely 16-1 and 16-2, are developed. To understand them fully, the reader must study the last five chapters of the book. A simpler approach would have been to provide in Chapter 16 more focused examples that exclude queuing theory, and to incorporate the present examples at the end of the book.

Some time ago, I was involved in the design of an integrated service digital network in a large plant. The main problem was getting an agreement between the telecommunication department and the computer department. Neither group had a complete understanding of the problems involved in the project. This book would have eased the relationship between these two factions, since the people of the telecommunication department would have learned more about controllers and multiplexers and how to deal with the channel and capacity problem, while the people from the computer department would have learned more about digital switching networks.

This is a good book for all those who want to familiarize themselves with the present state of the art in data communications. It is also a good reference book for students interested in this field, since it describes state of the art equipment in data communications and interconnection methodology not usually covered in detail.

Walter Grote
Polytechnic University, Brooklyn

Fuzzy Mathematical Techniques with Applications

Abraham Kandel (Addison-Wesley, Reading, Mass., 1986, 274 pp., $37.95)

This text provides a readable introduction to the basic theories of fuzzy mathematics and a comprehensive exposition of some of the main applications. The text is particularly recommended for specialists in applied mathematics and researchers in artificial intelligence. In AI implementation, topics such as common sense reasoning have eluded scientific treatment and formalization within the framework of classical logic and probability theory. Researchers in this field are encouraged by the ability of the theory of fuzzy sets to provide a formal basis for dealing with uncertainty in expert systems. The application of the theory of fuzzy sets to this problem may be the acid test that will determine the theory's practical usefulness.

Fuzzy set theory can be applied to expert systems.

Fuzzy set theory has its origins in a now classic 1965 article by Lotfi Zadeh of UC Berkeley (L. Zadeh, "Fuzzy Sets," *Information and Control*, Vol. 8, 1965, pp. 338-353). This article attracted wide interest and resulted in the rapid development of this unorthodox and controversial field. The theory of fuzzy subsets is based upon multivalued logic and allows us to entertain conflicting propositions. A key result, the Goguen representation theorem (J.A. Goguen, "L-Fuzzy Sets," *J. of Math. Analysis and Applications*, Vol. 18, 1967, pp. 145-174), states that any system satisfying certain axioms is equivalent to a system of fuzzy sets. The Goguen representation theorem is a precise mathematical result in the theory of categories. It allows us to conclude that inexact concepts can be represented by fuzzy sets.

The basic idea underlying fuzzy sets is that a subset A of the universe of discourse X (for example, the set A of beautiful persons in a town X) is such that the transition between full membership and no membership is gradual rather than abrupt. The more an object x belongs to A, the closer to 1 is its grade of membership $\chi_A(x)$, where the grade of membership 1 is assigned to those objects that fully belong to A while 0 is assigned to those objects that do not belong to A at all. A fuzzy set is thus a "class" with a continuum of grades of membership, and is a generalization of abstract nonfuzzy ("crisp") set theory where the grades of membership can only take the binary values 0 or 1. If $X = \{x\}$ denotes a space of objects, then a fuzzy set A in X is a set of ordered pairs $A = \{x, \chi_A(x)\}$ where $\chi_A(x)$ is termed "the grade of membership of x in A" and is a number in the interval [0,1]. The grades of membership reflect an "ordering" of the objects in the universe and can be interpreted as the degree of compatibility of the predicate associated with A and the object x.

The author observes that there are "three kinds of inexactness: generality, that a concept applies to a variety of situations; ambiguity, that it describes more than one distinguishable subconcept; and vagueness, that precise boundaries are not defined." He explains that each of the three types of inexactness can be represented by a fuzzy set and provides examples of how this is done.

The text consists of seven chapters and an extensive bibliography of some 1000 references. The chapter topics are "Fuzzy Sets," "Possibility Theory and Fuzzy Quantification," "Fuzzy Functions," "Fuzzy Events and Fuzzy Statistics," "Fuzzy Relations," "Fuzzy Logics," and "Some Applications."

The author of *Fuzzy Mathematical Techniques with Applications* conjectures that "Eventually, . . ., the theory of fuzzy sets is likely to be recognized as a natural development in the evolution of scientific thinking; and the skepticism about its usefulness will be viewed, in retrospect, as a manifestation of the human attachment to tradition and resistance to innovation." I concur with this conjecture and believe that his text does much to realize that end.

Frank Parkash Mathur
California State Polytechnic University

Computer-Aided Design and Manufacturing: Methods and Tools (2nd ed.)

U. Rembold and R. Dillman (eds.)
(Springer-Verlag, New York,
1986, 458 pp., $88.50)

This book is compiled from a series of lecture notes on computer-aided manufacturing at the University of Karlsruhe in 1983 and has recently been revised and enlarged. The eleven chapters, each a separate article, cover a broad range of topics including CAD, computer-integrated manufacturing, robotics, and machine vision. The material on computer-aided design and manufacturing is advanced enough to be used as reference material for a course in the discipline.

The book suffers from a number of serious limitations. The eleven chapters do not blend into a coherent, readable text. The overall organization, as well as the organization of the individual chapters, is poor and detracts from the contents. For example, the titles of most of the chapters and sections do not accurately reflect their contents. In a few cases, the titles are irrelevant and misleading. Often, they are long, difficult to grasp, and refer to the original lectures rather than the actual chapter content (for example, "Design Methodology of Computer Integrated Manufacturing and Control of Manufacturing Units").

The content of particular chapters is often sketchy and inconsistent. One would expect each chapter to provide a detailed description of the basics of an advanced technique and then provide the details of its different methods and tools. In fact, the basics are often missing, and the details of the specific methods are so sketchy that the reader is unable to extrapolate the basics. Instead of details about an advanced technique, the reader is likely to find a history of where the technique was developed, a sketchy description of the technique, and a reference to an obscure paper. While some chapters are intended for engineers and scientists, others seem to be intended for the management type who may not be interested in details.

Another serious problem is the indiscriminate use of acronyms. This practice causes a good deal of frustration and confusion. In addition, figures are often not accompanied by any explanatory text, leaving the reader confused. The references in some chapters to "this paper" are misleading and obviously remain from the original articles. Transitions between adjacent sections and chapters are very difficult to follow, and the conclusions of most chapters are not found at the end of the chapter that they belong to, but at the end of the previous section.

If one can read through all these barriers, the book is quite rich in its presentation of advanced techniques and tools. The articles: "Quality Assurance and Machine Vision for Inspection" by P. Levi, "Production Control and Information Systems" by A. Scheer, and "Economic Analysis of Computer-Integrated Manufacturing Systems" by F. Leimkuhler are delightful and stimulating. The chapter "Present State and Future Trends in the Development of Programming Languages for Manufacturing" by U. Rembold and W. Epple provides good insight, although the section on commercial data processing seems irrelevant and out of place. R. Dillman's article, "Computing Aids to Plan and Control Manufacturing," is well written except that the section on the fifth-generation computer architecture does not belong in the chapter. More details on the graphical simulation techniques would improve the reader's understanding.

The book presents a variety of advanced CAD techniques and tools.

In "Programming of Robot Systems" by G.Gini et al., the reference to the Ada language is out of date. Also, the reader is left wondering why a section on programming a manipulation system is missing and why there is no discussion of the basics of programming a vision system. Although machine vision is discussed in this chapter, it appears in a section different than the one suggested by the titles. The criteria for classifying robot-programming languages are never discussed although the topic appears in one of the section titles. However, the section on error recovery is valuable.

Overall, the positive aspects of this book outweigh its negative aspects. As a reference book, it would make a worthwhile addition to computer science and electrical engineering libraries.

Sumit Ghosh
AT&T Bell Laboratories

Kermit: A File Transfer Protocol

Frank da Cruz (Digital Press, Bedford, Mass., 1987, 379 pp., $25.00)

Kermit is a protocol for connecting computers and enabling the transfer of data between them. What makes Kermit interesting is that it is in the public domain: it is perfectly legal for you to copy the software from any place you can, although the Columbia University Computer Science Department likes to act as a central clearinghouse for the various implementations. Not surprisingly, the author is one of the people at Columbia who is active in this endeavor.

Upon reading the title of this book, you might ask, "Okay, this book is about that Kermit protocol, but will it tell me what I want to know about how to use the protocol?" Chances are that it will. In fact, the author could have called the book *Everything You Wanted to Know about Kermit, But Were Afraid to Ask*! It addresses the needs of a full spectrum of users, from the computer semiliterate who has only used "canned" programs, to the experienced user who merely wants to learn the Kermit command set, to the programmer who wants to implement Kermit on a new computer. Moreover, *Kermit: A File Transfer Protocol* is a friendly book that puts you at ease with amusing and informative illustrations.

The author has organized the book for selective reading. Chapter 1 ("Introduction") provides an introduction to the Kermit program. Chapter 2 ("The Basics") and Chapter 3 ("Computers and Files") answer some of the fundamental issues that concern the reader who is worried that he doesn't know enough to use Kermit. Chapter 4 ("Data Communications") provides a good crash course in data communications. This chapter also gives you a feel for the problems involved in hooking several boxes together serially and trying to get the end ones to talk together without interruption. Chapters 5-7 ("User Guide") provide the mainstream computer programmer with the necessary information to get Kermit working quickly. Chapters 8-13 ("Programmer Guide") provide programming information for the ambitious developer.

For people who are itching to get started right away, the book provides 12 pages of sample sessions between some of the most commonly connected computer types. The book also provides good help on building your own connecting cables and debugging them. This information may be all you need to try out the system and get a feel for how Kermit works.

The author even goes so far as to provide an MS-DOS Basic program that could help you read the Kermit source over to your machine via the PC's RS-232-C port. The program is an implementation of a simple subset of Kermit and is appropriately deemed a "bootstrapping" technique.

Throughout the book, the author demonstrates that his understanding of current computing and programming is more than sufficient to write this text. In fact, he sometimes goes into much more detail than the majority of his audience will probably need. For example, in Chapter 3 he provides variations on the ASCII code and different ways that records or lines are terminated. These are details that most casual users will never need to know, as long as they have competent support staff who can set things up right from the start. Also, his instructions on proper use of modems may be too detailed, considering that nowadays modems come with pretty good instruction manuals. (While on the subject of modems, I am sorry to say that the author makes the classic mistake of referring to bit rates in terms of "baud" rather than "bits per second.")

I will refrain from making any judgements on the Programmer Guide until I have taken the time to follow the instructions and write my own version of the Kermit protocol. For the other applications, however, I strongly recommend the book, even though some sections of the book may prove unnecessary for your particular needs.

James Heliotis
Rochester Institute of Technology

Becoming a Technical Leader: An Organic Problem-Solving Approach

Gerald M. Weinberg (Dorset House Publishing, New York, 1986, 284 pp., $29.50)

Much of the work in any technical or scientific arena is performed by projects, teams, or tightly bound task groups. Imagine a team of four researchers brainstorming over a complex problem: Together they might represent twenty-five or thirty years of university-level training on the subject area under discussion, and precisely zero years of training on team interaction. Yet any breakthroughs in solving the problem may be as much due to successful interaction as to the subject-area expertise of the individuals.

We spend all day, every day thinking, but almost no time thinking about thinking. We interact for hours of every work day, but almost never is the subject of our interaction the interaction itself. Gerald Weinberg, in his always fascinating *Becoming a Technical Leader*, sets out to right some of these imbalances. He focuses our attention on what it takes to make teams of thinking technical people work effectively together.

The crucial ingredient is leadership. One moment the team is stalled, then suddenly it isn't. What has occurred in the interval is an act of leadership—some team member has gotten the thought process working again. Weinberg makes a distinction between the person that does this (the leader) and the person appointed to be in charge (the "Leader"). He points out that much of what is written about leadership is really about "Leadership" or "Managership." But leading and managing are very different things. The leadership that matters most is not that which comes from our appointed supervisors, but rather the momentary leadership supplied by peers. When this process works well, we seldom even notice it. When it works poorly, or not at all, the work comes to a grinding halt.

Weinberg goes over the classes of leadership acts, the pathologies that stop us from leading effectively or cause us to thwart the leadership of others, and the positive actions we can take to make things better. All of this he does with a gentle humor and candor.

The strongest part of *Becoming a Technical Leader* is its central section on the mechanics of interaction. Weinberg takes a simple two-sentence interchange between teammates and analyzes it in a level of detail that leaves you stunned and wondering "How could so much have been going on beneath the surface?" But, surprising as the analysis is, you don't doubt it for a second. The author leads you step by step toward conclusions that are astonishing but inevitable.

When you pause at the end of such a chapter, you're liable to conclude that you have been changed by what you've read. Weinberg not only writes convincingly about being a leader—he is one.

Tom DeMarco
The Atlantic Systems Guild

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Instructions: Submit five copies to the Program Chairman by March 14, 1988. Papers must be in English, be typed double-spaced, and not exceed 25 pages (about 5000 words). Papers must have: ■ a title page that lists the name, mailing and electronic address, and telephone number for each author; ■ an abstract; ■ keywords; ■ and the presentation media requirement. For multiple author papers, identify the corresponding author and the presenting author.

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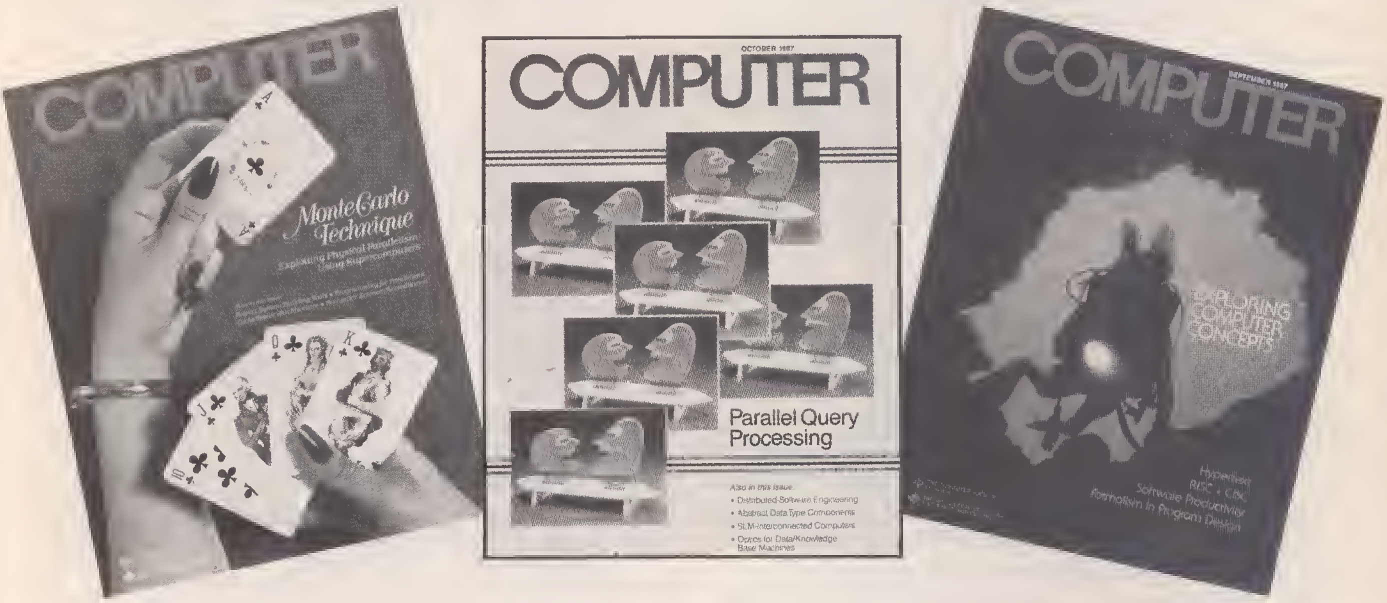
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6	26	46	66	86	106	126	146	166	186
7	27	47	67	87	107	127	147	167	187
8	28	48	68	88	108	128	148	168	188
9	29	49	69	89	109	129	149	169	189
10	30	50	70	90	110	130	150	170	190
11	31	51	71	91	111	131	151	171	191
12	32	52	72	92	112	132	152	172	192
13	33	53	73	93	113	133	153	173	193
14	34	54	74	94	114	134	154	174	194
15	35	55	75	95	115	135	155	175	195
16	36	56	76	96	116	136	156	176	196
17	37	57	77	97	117	137	157	177	197
18	38	58	78	98	118	138	158	178	198
19	39	59	79	99	119	139	159	179	199
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12	32	52	72	92	112	132	152	172	192
13	33	53	73	93	113	133	153	173	193
14	34	54	74	94	114	134	154	174	194
15	35	55	75	95	115	135	155	175	195
16	36	56	76	96	116	136	156	176	196
17	37	57	77	97	117	137	157	177	197
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- Parallel Algorithms
- Applications

Emerging Technologies
- Intelligent Processing
- Customized Knowledge Based Systems
- Intelligent Software Development Support Systems
- Intelligent Human Interface
- Wide Area Network Management

DEADLINES:

- February 15, 1988 for receiving all papers and proposals
- March 15, 1988 panel organizer notified of acceptance
- April 1, 1988 organizers of accepted panel proposals provide final information on session chairmen and panelists
- April 25, 1988 authors notified of acceptance
- June 15, 1988 camera-ready copies of accepted papers and panelists position papers due.

INFORMATION FOR AUTHORS:

- 5 copies of the full paper (double spaced) 1000-5000 words
- Proposals should include: title, organizer/affiliations/address/phone and 150-word abstract

INFORMATION FOR PANEL ORGANIZERS:

- 5 copies of the panel proposal
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